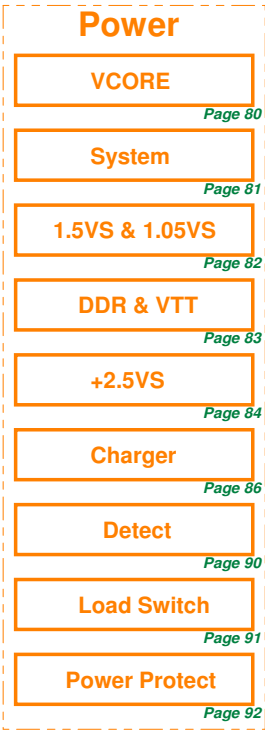
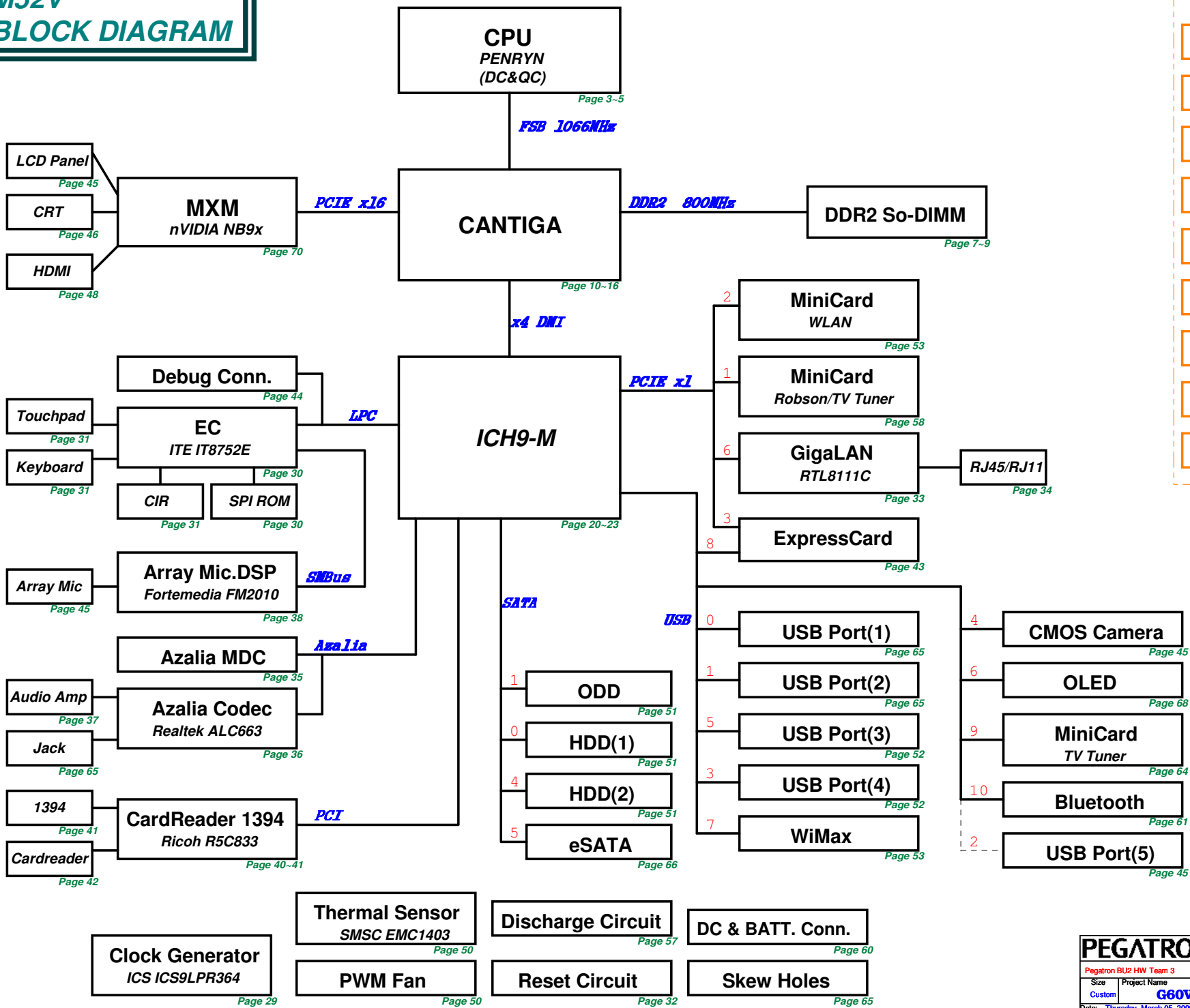


M52V BLOCK DIAGRAM



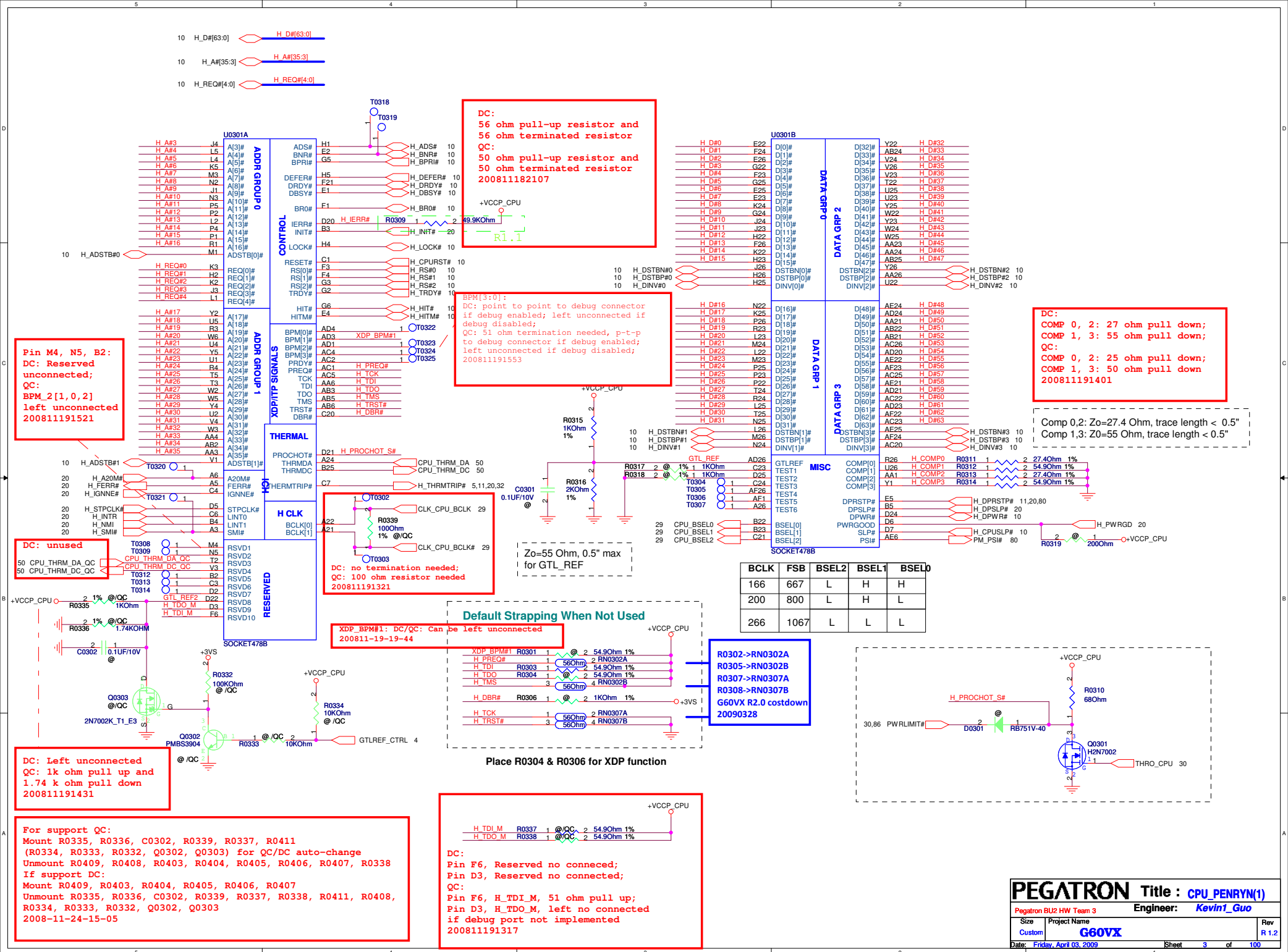
ICH9-M GPIO SETTING

Pin	Pin Name	Signal Name	Type
AG12	BM_BUSY#/GPIO0	PM_BMBUSY#	I
AJ8	TACH1/GPIO1	BT_DECT#	I
F8	PIRQE#/GPIO2	PCI_INTE#	I/OD
G11	PIRQF#/GPIO3	PCI_INTF#	I/OD
F12	PIRQG#/GPIO4	PCI_INTG#	I/OD
B3	PIRQH#/GPIO5	PCI_INTH#	I/OD
AJ9	TACH2/GPIO6		
AH9	TACH3/GPIO7	WLAN_LED_ON	O
AE16	GPIO8	EXT_SMI#	I
AG19	WOL_EN/GPIO9		
AJ24	CLGPIO1/GPIO10		
AG22	SMBALERT#/GPIO11	SMB_ALERT#	I
AC19	GPIO12	EXT_SCI#	I
AH21	GLAN_DOCK#/GPIO13		
AF22	CLGPIO2/GPIO14		
AE20	STP_PC#/GPIO15	STP_PC#	I/O
AJ14	DPRSLPVR/GPIO16	PM_DPRSLPVR	O
AG8	TACH0/GPIO17	WLAN_ON#	O
AH12	GPIO18		
AJ10	GPIO19/SATA1GP		
AE11	GPIO20	BT_LED_ON	O
AJ12	SATA0GP/GPIO21		
AG10	SCLOCK/GPIO22		
E6	LDRQ1#/GPIO23		
AJ27	CLGPIO0/GPIO24		
AG18	STP_CPU#/GPIO25	STP_CPU#	O
AH27	S4_STATE#/GPIO26		
AH25	QRT_STATE0/GPIO27	BT_ON#	O
AD16	QRT_STATE1/GPIO28	CB_SD#	O
AG17	OC#5/GPIO29	INT_USB_OC#	I
AD12	OC#6/GPIO30	INT_USB_OC#	I
AJ18	OC#7/GPIO31	INT_USB_OC#	I
AH11	CLKRUN#/GPIO32	PM_CLKRUN#	O
AE10	AZ_DOCK_EN#/GPIO33		
AG14	AZ_DOCK_RST#/GPIO34		
AG13	SATACLKREQ#/GPIO35		
AF11	SATA2GP/GPIO36	EMAIL_LED#	O
AG11	SATA3GP/GPIO37	PCB_ID0	I
AF9	SLOAD/GPIO38	PCB_ID1	I
AJ11	SDATAOUT0/GPIO39	PCB_ID2	I
AG16	OC#1/GPIO40	USB_CON01_OC#	I
AG15	OC#2/GPIO41	USB_CON23_OC#	I
AE15	OC#3/GPIO42	USB_CON23_OC#	I
AF15	OC#4/GPIO43	NEWCARD_OC#	I
AD10	SATAOUT1/GPIO48		
AG29	CPUPWRGD/GPIO49	H_PWRGD	O
E18	REQ1#/GPIO50	PCI_REQ#1	I/O
C18	GNT1#/GPIO51		
B19	REQ2#/GPIO52	PCI_REQ#2	I/O
F18	GNT2#/GPIO53		
A11	REQ3#/GPIO54	PCI_REQ#3	I/O
C10	GNT3#/GPIO55		

EC IT8512E GPIO SETTING

Pin	Pin Name	Signal Name	Type	Pin	Pin Name	Signal Name	Type
28	PWM0/GPA0	PWR_LED_UP#	O	105	CLKRUN#/GPH0	PM_CLKRUN#	I/O
29	PWM1/GPA1	CHG_LED_UP#	O	106	CRX1/GPH1	3G_ON#	O
32	PWM2/GPA2			107	CTX1/GPH2	3G_LED_ON#	O
33	PWM3/GPA3			108	GPH3	BAT_LEARN	I/O
34	PWM4/GPA4	LCD_BL_PWM	O	109	GPH4		
35	PWM5/GPA5	FAN_PWM	O	110	GPH5	NUM_LED	O
36	PWM6/GPA6			111	GPH6	CAP_LED	O
38	PWM7/GPA7			74	ADC0/GPI0	NV_OVERT#	I
122	RXD/GPB0	CHG_EN#	O	75	ADC1/GPI1	SUS_PWRGD	I
123	TXD/GPB1	PRECHG	O	76	ADC2/GPI2	ALL_SYS_PWRGD	I
139	CTX0/GPB2			77	ADC3/GPI3	CPU_PWRGD	I
124	SMCLK0/GPB3	SMB0_CLK	I/O	78	ADC4/GPI4	PWR_MON	I
125	SMDAT0/GPB4	SMB0_DAT	I/O	79	ADC5/GPI5	ALS_DA	I
142	GA20/GPB5	A20GATE	O	80	ADC6/GPI6		
4	KBRST#/GPB6	RC_IN#	O	81	ADC7/GPI7		
126	GPB7	PM_RSMRST#	O	84	DAC0/GPJ0	EC_CLK_EN	
133	CRX0/GPC0	CRX0	I	85	DAC1/GPJ1	PM_PWROK	
129	SMCLK1/GPC1	SMB1_CLK	I/O	86	DAC1/GPJ2		
130	SMDAT1/GPC2	SMB1_DAT	I/O	87	DAC1/GPJ3		
64	GPC3	PM_PWRBTN#	O	88	DAC1/GPJ4		
136	WUI2/GPC4	AC_IN_OC#	I	89	DAC1/GPJ5		
65	GPC5	OP_SD#	O	15	GPK0		
140	WUI3/GPC6	BAT1_IN_OC#	I	16	GPK1		
20	GPC7	RFON_SW#	I	17	GPK2		
22	WUI0/GPD0	PWRLIMIT#	I	18	GPK3		
25	WUI1/GPD1	PM_SUSC#	I	48	GPK4		
26	WUI4/GPD2	BUF_PLT_RST#	I	49	GPK5		
27	ECSCI#/GPD3	EXT_SCI#	O	62	GPK6		
19	GPD4	EXT_SMI#	O	63	GPK7		
37	GPD5	LCD_BACKOFF#	O	90	GPL0		
53	TACH0 / GPD6	FAN0_TACH	I	91	GPL1		
54	GPD7			92	GPL2		
23	GPE0	VSUS_ON	O	93	GPL3		
94	GPE1	SUSC_EC#	O	119	GPL4		
95	GPE2	SUSB_EC#	O	120	GPL5		
96	GPE3	CPU_VRON	O	134	GPL6		
141	PWRSW/GPE4	PWR_SW#	I	135	GPL7		
39	WUI5/GPE5	BAT2_IN_OC#	I				
21	GPE6	LID_SW#	I				
24	GPE7	INSTANT_ON#	I				
97	PS2CLK0/GPF0						
98	PS2DAT0/GPF1	COLOREN#	I				
99	PS2CLK1/GPF2	MARATHON#	I				
100	PS2DAT1/GPF3	DISTP#	I				
101	PS2CLK2/GPF4	TP_CLK	I/O				
102	PS2DAT2/GPF5	TP_DAT	I/O				
131	SMCLK2/GPF6	THRO_CPU	O				
132	SMDAT2/GPF7	TP_LED	O				
118	WUI7/GPG0						
121	GPG1	PM_SUSB#	I				
112	GPG2						
116	GPG6						

PEGATRON		Title : System Setting	
Pegatron BU2 HW Team 3		Engineer: Kevin1_Guo	
Size	Project Name	Rev	
Custom	G60VX	R 1.2	
Date: Thursday, March 05, 2009		Sheet	2 of 100



+V CORE

+V CORE

U0301C

A7

A9

A10

A12

A13

A15

A17

A18

A20

B7

B9

B10

B12

B14

B15

B17

B18

B20

C9

C10

C12

C13

C15

C17

C18

D9

D10

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AA7

AA9

AA10

AA12

AA13

AA15

AA17

AA18

AA20

AB9

AC10

AB10

AB12

AB14

AB15

AB17

AB18

VCC68

VCC69

VCC70

VCC71

VCC72

VCC73

VCC74

VCC75

VCC76

VCC77

VCC78

VCC79

VCC80

VCC81

VCC82

VCC83

VCC84

VCC85

VCC86

VCC87

VCC88

VCC89

VCC90

VCC91

VCC92

VCC93

VCC94

VCC95

VCC96

VCC97

VCC98

VCC99

VCC100

VCCP1

VCCP2

VCCP3

VCCP4

VCCP5

VCCP6

VCCP7

VCCP8

VCCP9

VCCP10

VCCP11

VCCP12

VCCP13

VCCP14

VCCP15

VCCP16

VCCA1

VCCA2

VCC54

VCC55

VCC56

VCC57

VCC58

VCC59

VCC60

VCC61

VCC62

VCC63

VCC64

VCC65

VCC66

VCC67

VCC68

VCC69

VCC70

VCC71

VCC72

VCC73

VCC74

VCC75

VCC76

VCC77

VCC78

VCC79

VCC80

VCC81

VCC82

VCC83

VCC84

VCC85

VCC86

VCC87

VCC88

VCC89

VCC90

VCC91

VCC92

VCC93

VCC94

VCC95

VCC96

VCC97

VCC98

VCC99

VCC100

VCCP1

VCCP2

VCCP3

VCCP4

VCCP5

VCCP6

VCCP7

VCCP8

VCCP9

VCCP10

VCCP11

VCCP12

VCCP13

VCCP14

VCCP15

VCCP16

VCCA1

VCCA2

VCC54

VCC55

VCC56

VCC57

VCC58

VCC59

VCC60

VCC61

VCC62

VCC63

VCC64

VCC65

VCC66

VCC67

VCC68

VCC69

VCC70

VCC71

VCC72

VCC73

VCC74

VCC75

VCC76

VCC77

VCC78

VCC79

VCC80

VCC81

VCC82

VCC83

VCC84

VCC85

VCC86

VCC87

VCC88

VCC89

VCC90

VCC91

VCC92

VCC93

VCC94

VCC95

VCC96

VCC97

VCC98

VCC99

VCC100

VCCP1

VCCP2

VCCP3

VCCP4

VCCP5

VCCP6

VCCP7

VCCP8

VCCP9

VCCP10

VCCP11

VCCP12

VCCP13

VCCP14

VCCP15

VCCP16

VCCA1

VCCA2

VCC54

VCC55

VCC56

VCC57

VCC58

VCC59

VCC60

VCC61

VCC62

VCC63

VCC64

VCC65

VCC66

VCC67

VCC68

VCC69

VCC70

VCC71

VCC72

VCC73

VCC74

VCC75

VCC76

VCC77

VCC78

VCC79

VCC80

VCC81

VCC82

VCC83

VCC84

VCC85

VCC86

VCC87

VCC88

VCC89

VCC90

VCC91

VCC92

VCC93

VCC94

VCC95

VCC96

VCC97

VCC98

VCC99

VCC100

VCCP1

VCCP2

VCCP3

VCCP4

VCCP5

VCCP6

VCCP7

VCCP8

VCCP9

VCCP10

VCCP11

VCCP12

VCCP13

VCCP14

VCCP15

VCCP16

VCCA1

VCCA2

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VCC58

VCC59

VCC60

VCC61

VCC62

VCC63

VCC64

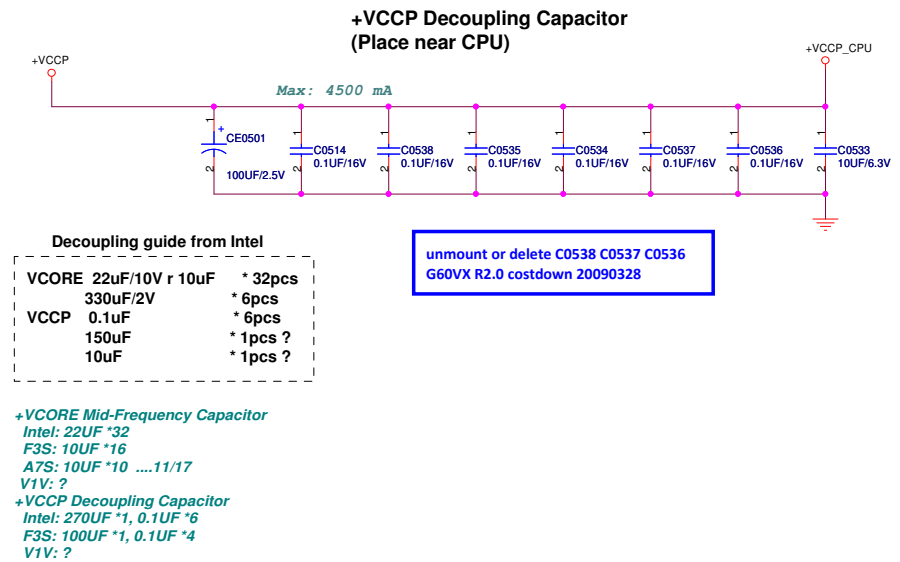
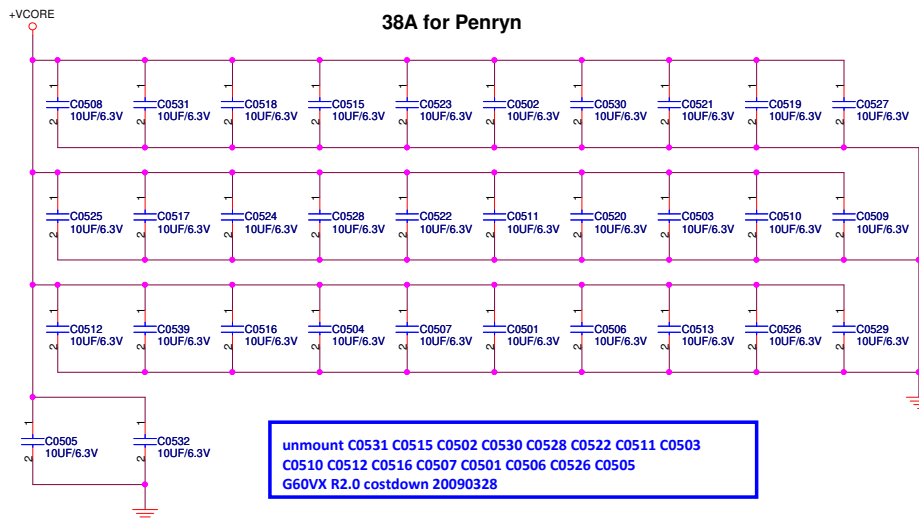
VCC65

VCC66

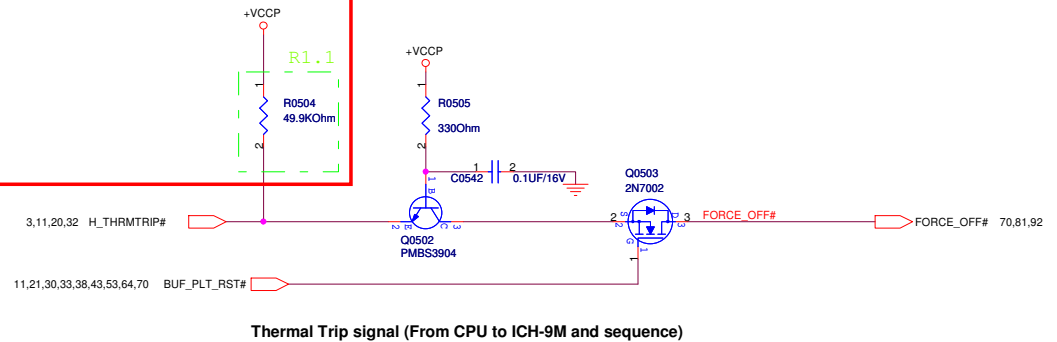
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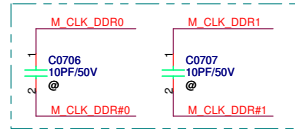
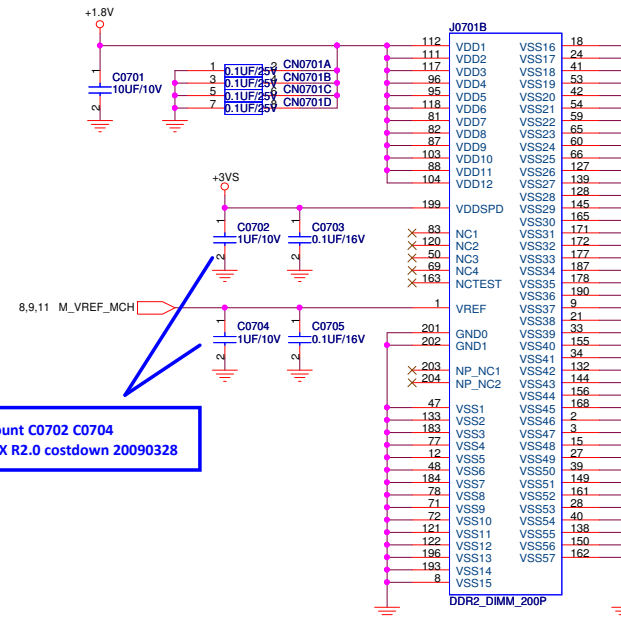
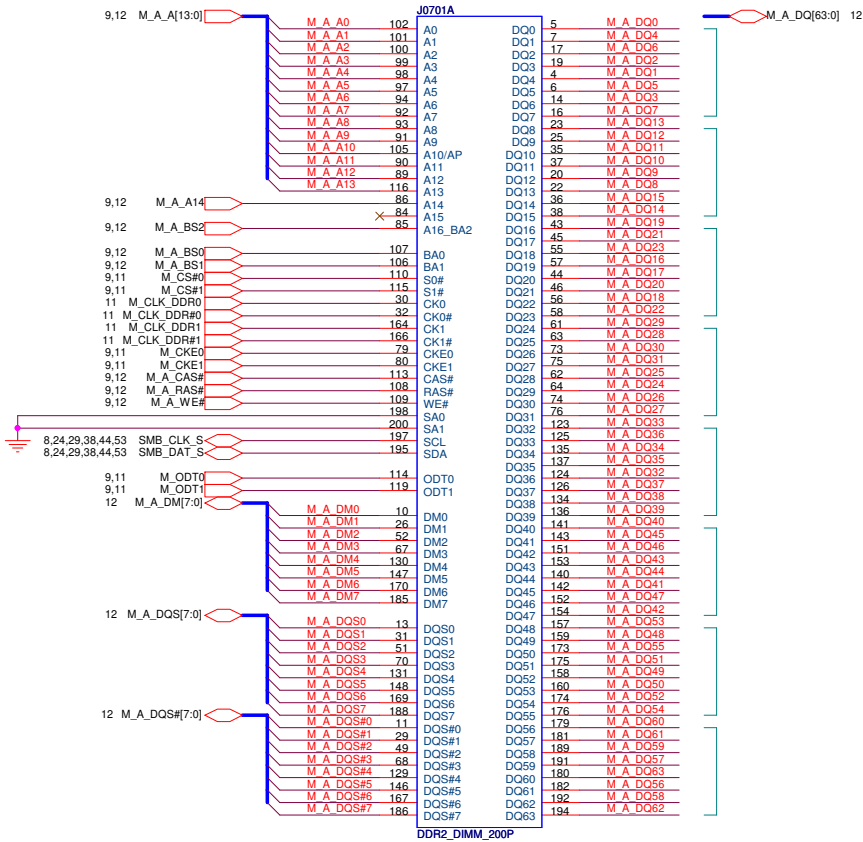


Checklist recommends THERMTRIP# pull up in the CPU side although functionality not used;
DC: 56 ohm pull up, 55 ohm terminate;
QC: 50 ohm pull up, 50 ohm terminate
200811190902

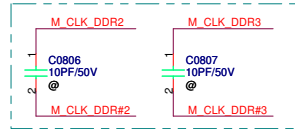
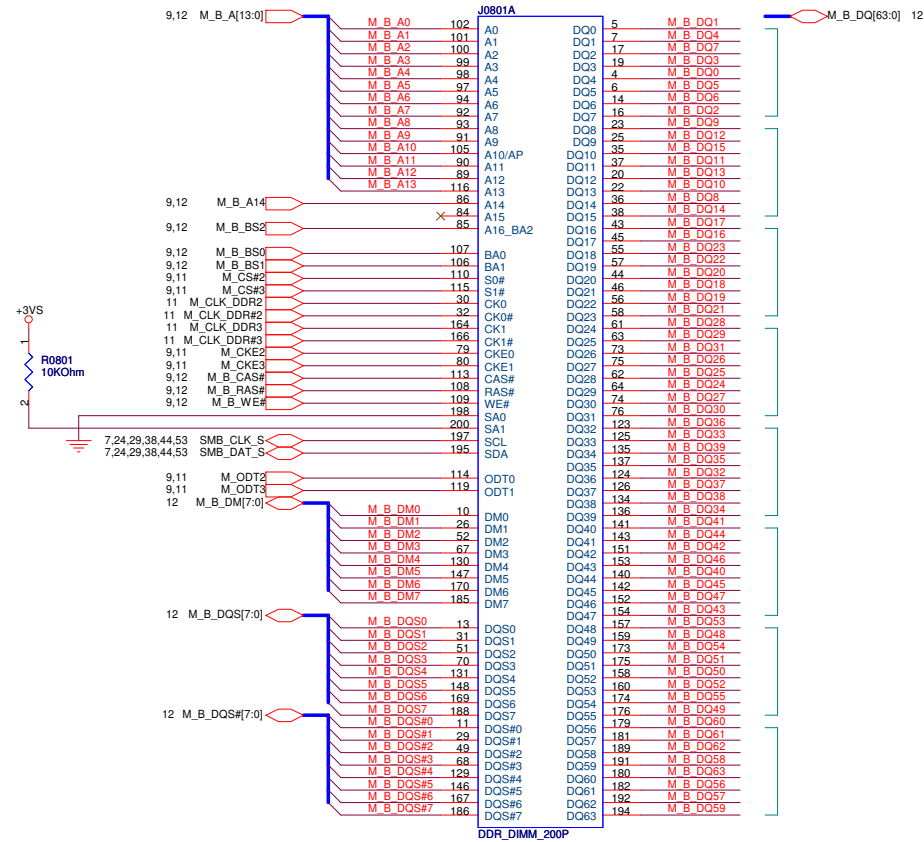


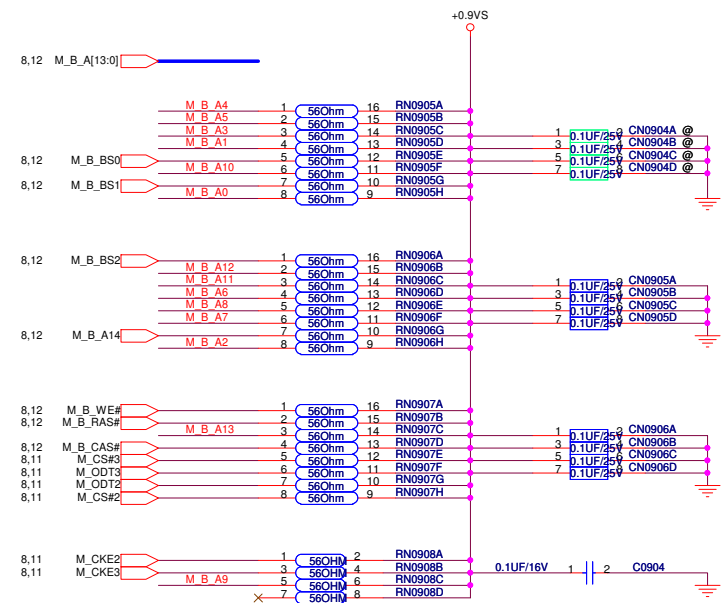
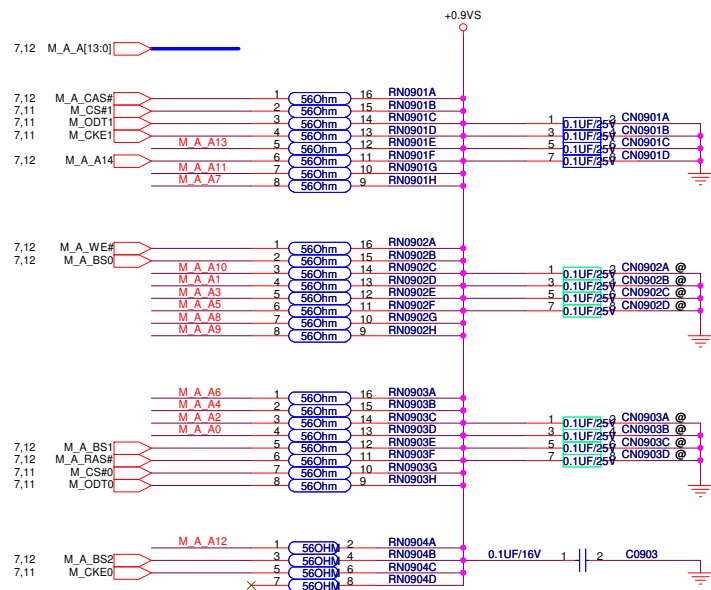
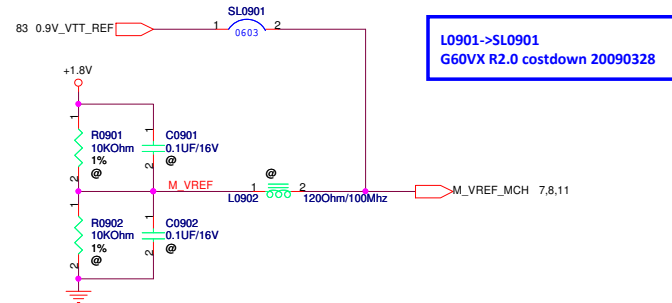
PEGATRON		Title : CPU ****	
Pegatron BU2 HW Team 3		Engineer: Kevin1_Guo	
Size	Project Name		Rev
Custom	G60VX		R 1.2
Date: Thursday, March 05, 2009		Sheet	6 of 100

Reserved for 3G

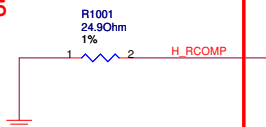
Reverse Type
H = 9.2 mm

Reserved for 3G

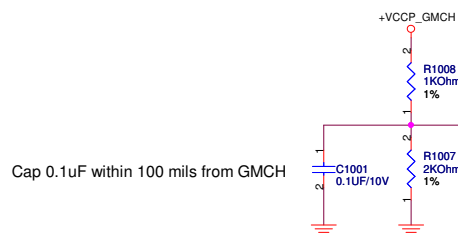
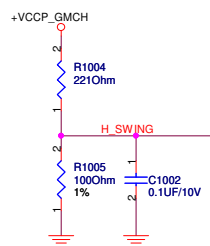
Reverse Type
H = 4.0 mm



DC: 25 ohm pull down;
QC: 17 ohm pull down
2008-11-19-20-25



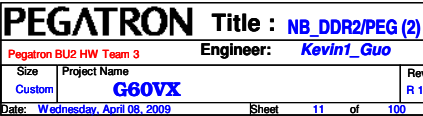
```
DC: 221 ohm pull up,  
100 ohm pull down;  
QC: 221 ohm pull up,  
75 ohm pull down  
2008-11-19-20-27
```



RX1006->SL1006;
G60VX R2.0 costdown 20090405

U001A					
H_D#0	F2	H_D#_0	H_A#3	A14	H_A#3
H_D#1	G8	H_D#_1	H_A#_4	C15	H_A#4
H_D#2	F8	H_D#_2	H_A#_5	F16	H_A#5
H_D#3	E8	H_D#_3	H_A#_6	H18	H_A#6
H_D#4	G2	H_D#_4	H_A#_7	C18	H_A#7
H_D#5	H6	H_D#_5	H_A#_8	M16	H_A#8
H_D#6	H2	H_D#_6	H_A#_9	J13	H_A#9
H_D#7	F6	H_D#_7	H_A#_10	P16	H_A#10
H_D#8	D4	H_D#_8	H_A#_11	R16	H_A#11
H_D#9	H3	H_D#_9	H_A#_12	N17	H_A#12
H_D#10	M1	H_D#_10	H_A#_13	M13	H_A#13
H_D#11	M11	H_D#_11	H_A#_14	E17	H_A#14
H_D#12	J1	H_D#_12	H_A#_15	P17	H_A#15
H_D#13	J2	H_D#_13	H_A#_16	F17	H_A#16
H_D#14	N12	H_D#_14	H_A#_17	G20	H_A#17
H_D#15	J6	H_D#_15	H_A#_18	B19	H_A#18
H_D#16	P2	H_D#_16	H_A#_19	J16	H_A#19
H_D#17	L2	H_D#_17	E20	H20	H_A#20
H_D#18	R2	H_D#_18	H_A#_21	E16	H_A#21
H_D#19	N9	H_D#_19	H_A#_22	J20	H_A#22
H_D#20	L6	H_D#_20	H_A#_23	A17	H_A#23
H_D#21	M5	H_D#_21	H_A#_24	L17	H_A#24
H_D#22	J3	H_D#_22	H_A#_25	B16	H_A#25
H_D#23	N2	H_D#_23	H_A#_26	L16	H_A#26
H_D#24	R1	H_D#_24	C21	C21	H_A#27
H_D#25	N5	H_D#_25	J17	J17	H_A#28
H_D#26	N6	H_D#_26	H_A#_28	H20	H_A#29
H_D#27	P13	H_D#_27	H_A#_29	B18	H_A#30
H_D#28	N8	H_D#_28	H_A#_30	K17	H_A#31
H_D#29	L7	H_D#_29	H_A#_31	B20	H_A#32
H_D#30	N10	H_D#_30	H_A#_32	F21	H_A#33
H_D#31	M3	H_D#_31	H_A#_33	K21	H_A#34
H_D#32	Y3	H_D#_32	H_A#_34	L20	H_A#35
H_D#33	AD14	H_D#_33	H_A#_35		
H_D#34	Y6	H_D#_34	H_ADS#	H12	H_ADS# 3
H_D#35	Y10	H_D#_35	H_ADSTB#_0	B16	H_ADSTB# 3
H_D#36	Y12	H_D#_36	H_ADSTB#_1	G17	H_ADSTB#1 3
H_D#37	Y14	H_D#_37	H_BNR#	A9	H_BNR# 3
H_D#38	Y7	H_D#_38	H_BPH#	E11	H_BPH# 3
H_D#39	W2	H_D#_39	H_BREQ#	G12	H_BRO# 3
H_D#40	AA8	H_D#_40	H_DEFER#	E9	H_DEFER# 3
H_D#41	Y9	H_D#_41	H_DBSY#	B10	H_DBSY# 3
H_D#42	AA13	H_D#_42	HPLL_CLK	AH7	CLK_MCH_BCLK 29
H_D#43	AA9	H_D#_43	H_DPWR#	AH6	CLK_MCH_BCLK# 29
H_D#44	AA11	H_D#_44	H_DRDY#	J11	H_DPWR# 3
H_D#45	AD17	H_D#_45	H_DRDY#	F9	H_DRDY# 3
H_D#46	AD10	H_D#_46	H_HIT#	H9	H_HIT# 3
H_D#47	AD13	H_D#_47	H_HIT#	E12	H_HIT# 3
H_D#48	AE12	H_D#_48	H_LOCK#	H11	H_LOCK# 3
H_D#49	AE9	H_D#_49	H_TRDY#	C9	H_TRDY# 3
H_D#50	AA2	H_D#_50			
H_D#51	AD8	H_D#_51			
H_D#52	AA3	H_D#_52			
H_D#53	AD3	H_D#_53			
H_D#54	AD7	H_D#_54	H_DINV#_0	J8	H_DINV#0 3
H_D#55	AE14	H_D#_55	H_DINV#_1	F3	H_DINV#1 3
H_D#56	AE3	H_D#_56	H_DINV#_2	Y13	H_DINV#2 3
H_D#57	AC1	H_D#_57	H_DINV#_3	Y1	H_DINV#3 3
H_D#58	AE3	H_D#_58			
H_D#59	AC3	H_D#_59	H_DSTBN#_0	L10	H_DSTBN#0 3
H_D#60	AE11	H_D#_60	H_DSTBN#_1	M7	H_DSTBN#1 3
H_D#61	AE8	H_D#_61	H_DSTBN#_2	AA5	H_DSTBN#2 3
H_D#62	AC2	H_D#_62	H_DSTBN#_3	AE6	H_DSTBN#3 3
H_D#63	AD6	H_D#_63			
			H_DSTBP#_0	L9	H_DSTBP#0 3
			H_DSTBP#_1	M8	H_DSTBP#1 3
			H_DSTBP#_2	AA6	H_DSTBP#2 3
			H_DSTBP#_3	AE5	H_DSTBP#3 3
			H_REQ#_0	B15	H_REQ#0
			H_REQ#_1	K13	H_REQ#1
			H_REQ#_2	F13	H_REQ#2
			H_REQ#_3	B13	H_REQ#3
			H_REQ#_4	B14	H

3 H_A#[35:3] H_A#[35:3]
3 H_REQ#[4:0] H_REQ#[4:0]
3 H_D#[63:0] H_D#[63:0]



7 M_A_DQ[0:63]

M A DQ0	AJ38	SA_DQ_0
M A DQ1	AJ41	SA_DQ_1
M A DQ2	AN38	SA_DQ_2
M A DQ3	AM38	SA_DQ_3
M A DQ4	AJ36	SA_DQ_4
M A DQ5	AJ40	SA_DQ_5
M A DQ6	AM44	SA_DQ_6
M A DQ7	AM42	SA_DQ_7
M A DQ8	AN43	SA_DQ_8
M A DQ9	AN44	SA_DQ_9
M A DQ10	AU40	SA_DQ_10
M A DQ11	AT38	SA_DQ_11
M A DQ12	AN41	SA_DQ_12
M A DQ13	AN39	SA_DQ_13
M A DQ14	AU44	SA_DQ_14
M A DQ15	AU42	SA_DQ_15
M A DQ16	AY39	SA_DQ_16
M A DQ17	AY44	SA_DQ_17
M A DQ18	BA40	SA_DQ_18
M A DQ19	BD43	SA_DQ_19
M A DQ20	AV41	SA_DQ_20
M A DQ21	AY43	SA_DQ_21
M A DQ22	BB41	SA_DQ_22
M A DQ23	BC40	SA_DQ_23
M A DQ24	AY37	SA_DQ_24
M A DQ25	BD38	SA_DQ_25
M A DQ26	AV37	SA_DQ_26
M A DQ27	AT36	SA_DQ_27
M A DQ28	AY38	SA_DQ_28
M A DQ29	BB38	SA_DQ_29
M A DQ30	AV36	SA_DQ_30
M A DQ31	AW36	SA_DQ_31
M A DQ32	BD13	SA_DQ_32
M A DQ33	AU11	SA_DQ_33
M A DQ34	BC11	SA_DQ_34
M A DQ35	BA12	SA_DQ_35
M A DQ36	AU13	SA_DQ_36
M A DQ37	AV13	SA_DQ_37
M A DQ38	BD12	SA_DQ_38
M A DQ39	BC12	SA_DQ_39
M A DQ40	BB9	SA_DQ_40
M A DQ41	BA9	SA_DQ_41
M A DQ42	AU10	SA_DQ_42
M A DQ43	AV9	SA_DQ_43
M A DQ44	BA11	SA_DQ_44
M A DQ45	BD9	SA_DQ_45
M A DQ46	AY8	SA_DQ_46
M A DQ47	BA6	SA_DQ_47
M A DQ48	AV5	SA_DQ_48
M A DQ49	AV7	SA_DQ_49
M A DQ50	AT9	SA_DQ_50
M A DQ51	AN8	SA_DQ_51
M A DQ52	AU5	SA_DQ_52
M A DQ53	AU6	SA_DQ_53
M A DQ54	AT5	SA_DQ_54
M A DQ55	AN10	SA_DQ_55
M A DQ56	AM11	SA_DQ_56
M A DQ57	AM5	SA_DQ_57
M A DQ58	AJ9	SA_DQ_58
M A DQ59	AJ8	SA_DQ_59
M A DQ60	AM12	SA_DQ_60
M A DQ61	AM13	SA_DQ_61
M A DQ62	AJ11	SA_DQ_62
M A DQ63	AJ12	SA_DQ_63

CANTIGA_CHIPSET

DDR SYSTEM MEMORY A

SA_BS_0	BD21	M_A_BS0 7.9
SA_BS_1	BQ18	M_A_BS1 7.9
SA_BS_2	AT25	M_A_BS2 7.9
SA_RAS#	BB20	M_A_RAS# 7.9
SA_CAS#	BD20	M_A_CAS# 7.9
SA_WE#	AY20	M_A_WE# 7.9
SA_DM_0	AM37	M_A_DM0
SA_DM_1	AT41	M_A_DM1
SA_DM_2	AY41	M_A_DM2
SA_DM_3	AU39	M_A_DM3
SA_DM_4	BB12	M_A_DM4
SA_DM_5	AY6	M_A_DM5
SA_DM_6	AT7	M_A_DM6
SA_DM_7	AJ5	M_A_DM7
SA_DQS_0	AJ44	M_A_DQS0
SA_DQS_1	AT44	M_A_DQS1
SA_DQS_2	BA43	M_A_DQS2
SA_DQS_3	RC37	M_A_DQS3
SA_DQS_4	AW12	M_A_DQS4
SA_DQS_5	BC8	M_A_DQS5
SA_DQS_6	AU8	M_A_DQS6
SA_DQS_7	AM7	M_A_DQS7
SA_DQS#_0	AJ43	M_A_DQS#0
SA_DQS#_1	AT43	M_A_DQS#1
SA_DQS#_2	BA44	M_A_DQS#2
SA_DQS#_3	BD37	M_A_DQS#3
SA_DQS#_4	AY12	M_A_DQS#4
SA_DQS#_5	BD8	M_A_DQS#5
SA_DQS#_6	AU9	M_A_DQS#6
SA_DQS#_7	AM8	M_A_DQS#7
SA_MA_0	BA21	M_A_A0
SA_MA_1	BC24	M_A_A1
SA_MA_2	BH24	M_A_A2
SA_MA_3	BQ25	M_A_A3
SA_MA_4	BA24	M_A_A4
SA_MA_5	BD24	M_A_A5
SA_MA_6	RF25	M_A_A6
SA_MA_7	AW24	M_A_A7
SA_MA_8	BC21	M_A_A8
SA_MA_9	BQ26	M_A_A9
SA_MA_10	BH26	M_A_A10
SA_MA_11	BH17	M_A_A11
SA_MA_12	AY25	M_A_A12
SA_MA_13		
SA_MA_14		

M_A_DM[0:7] 7

M_A_DQS[0:7] 7

M_A_DQS#[0:7] 7

M_A_A[0:14] 7.9

8 M_B_DQ[0:63]

M B DQ0	AK47	SB_DQ_0
M B DQ1	AH46	SB_DQ_1
M B DQ2	AP47	SB_DQ_2
M B DQ3	AP46	SB_DQ_3
M B DQ4	AJ46	SB_DQ_4
M B DQ5	AJ46	SB_DQ_5
M B DQ6	AM48	SB_DQ_6
M B DQ7	AP48	SB_DQ_7
M B DQ8	AU47	SB_DQ_8
M B DQ9	AU46	SB_DQ_9
M B DQ10	BA46	SB_DQ_10
M B DQ11	AY48	SB_DQ_11
M B DQ12	AT47	SB_DQ_12
M B DQ13	AR47	SB_DQ_13
M B DQ14	AA47	SB_DQ_14
M B DQ15	BC47	SB_DQ_15
M B DQ16	BC46	SB_DQ_16
M B DQ17	BC44	SB_DQ_17
M B DQ18	BC43	SB_DQ_18
M B DQ19	BF43	SB_DQ_19
M B DQ20	BE45	SB_DQ_20
M B DQ21	BC41	SB_DQ_21
M B DQ22	BF40	SB_DQ_22
M B DQ23	BF41	SB_DQ_23
M B DQ24	BG38	SB_DQ_24
M B DQ25	BF38	SB_DQ_25
M B DQ26	BH35	SB_DQ_26
M B DQ27	BG35	SB_DQ_27
M B DQ28	BH40	SB_DQ_28
M B DQ29	BG39	SB_DQ_29
M B DQ30	BG34	SB_DQ_30
M B DQ31	BH34	SB_DQ_31
M B DQ32	BH14	SB_DQ_32
M B DQ33	BG12	SB_DQ_33
M B DQ34	BH11	SB_DQ_34
M B DQ35	BG8	SB_DQ_35
M B DQ36	BH12	SB_DQ_36
M B DQ37	BF11	SB_DQ_37
M B DQ38	BF8	SB_DQ_38
M B DQ39	BG7	SB_DQ_39
M B DQ40	BC5	SB_DQ_40
M B DQ41	BC6	SB_DQ_41
M B DQ42	AV3	SB_DQ_42
M B DQ43	AY1	SB_DQ_43
M B DQ44	BF6	SB_DQ_44
M B DQ45	BF5	SB_DQ_45
M B DQ46	BA1	SB_DQ_46
M B DQ47	BD3	SB_DQ_47
M B DQ48	AV2	SB_DQ_48
M B DQ49	AU3	SB_DQ_49
M B DQ50	AR3	SB_DQ_50
M B DQ51	AN2	SB_DQ_51
M B DQ52	AY2	SB_DQ_52
M B DQ53	AV1	SB_DQ_53
M B DQ54	AP3	SB_DQ_54
M B DQ55	AR1	SB_DQ_55
M B DQ56	AL1	SB_DQ_56
M B DQ57	AL2	SB_DQ_57
M B DQ58	AJ1	SB_DQ_58
M B DQ59	AH1	SB_DQ_59
M B DQ60	AM2	SB_DQ_60
M B DQ61	AM3	SB_DQ_61
M B DQ62	AH3	SB_DQ_62
M B DQ63	AJ3	SB_DQ_63

CANTIGA_CHIPSET

DDR SYSTEM MEMORY B

SB_BS_0	BC16	M_B_BS0 8.9
SB_BS_1	BB17	M_B_BS1 8.9
SB_BS_2	BB33	M_B_BS2 8.9
SB_RAS#	AU17	M_B_RAS# 8.9
SB_CAS#	BG16	M_B_CAS# 8.9
SB_WE#	BF14	M_B_WE# 8.9
SB_DM_0	AM47	M_B_DM0
SB_DM_1	AY47	M_B_DM1
SB_DM_2	BD40	M_B_DM2
SB_DM_3	BF35	M_B_DM3
SB_DM_4	BG11	M_B_DM4
SB_DM_5	BA3	M_B_DM5
SB_DM_6	AP1	M_B_DM6
SB_DM_7	AK2	M_B_DM7
SB_DQS_0	AL47	M_B_DQS0
SB_DQS_1	AV48	M_B_DQS1
SB_DQS_2	BG41	M_B_DQS2
SB_DQS_3	BG37	M_B_DQS3
SB_DQS_4	BH9	M_B_DQS4
SB_DQS_5	BB2	M_B_DQS5
SB_DQS_6	AU1	M_B_DQS6
SB_DQS_7	AN6	M_B_DQS7
SB_DQS#_0	AL46	M_B_DQS#0
SB_DQS#_1	AV47	M_B_DQS#1
SB_DQS#_2	BH41	M_B_DQS#2
SB_DQS#_3	BH37	M_B_DQS#3
SB_DQS#_4	BG9	M_B_DQS#4
SB_DQS#_5	BC2	M_B_DQS#5
SB_DQS#_6	AT2	M_B_DQS#6
SB_DQS#_7	AN5	M_B_DQS#7
SB_MA_0	AV17	M_B_A0
SB_MA_1	BA25	M_B_A1
SB_MA_2	BC25	M_B_A2
SB_MA_3	AU25	M_B_A3
SB_MA_4	AW25	M_B_A4
SB_MA_5	BB28	M_B_A5
SB_MA_6	AU28	M_B_A6
SB_MA_7	AT33	M_B_A7
SB_MA_8	BD33	M_B_A8
SB_MA_9	BB16	M_B_A9
SB_MA_10	AW33	M_B_A10
SB_MA_11	AY33	M_B_A11
SB_MA_12	BH15	M_B_A12
SB_MA_13	AU33	M_B_A13
SB_MA_14		

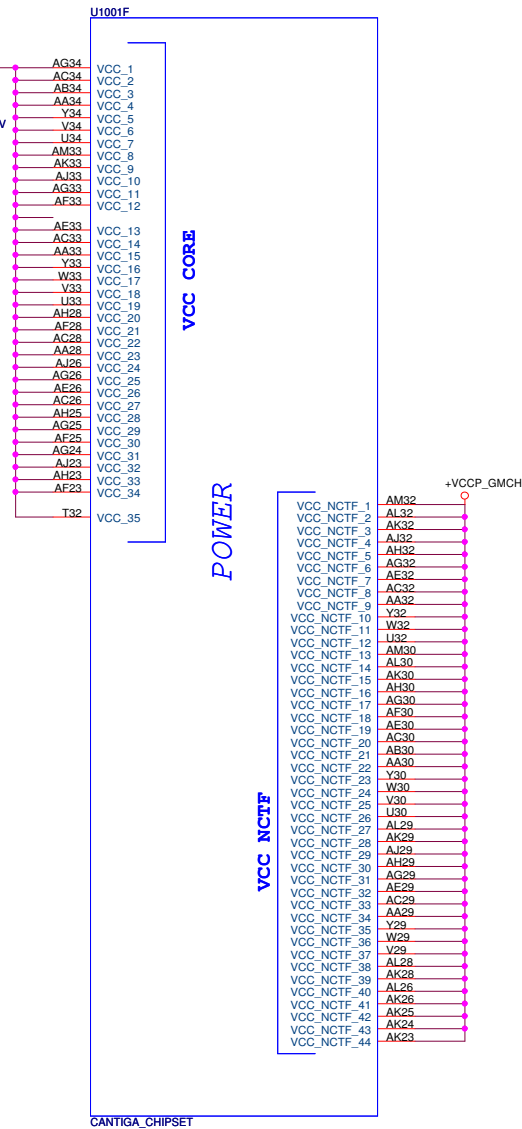
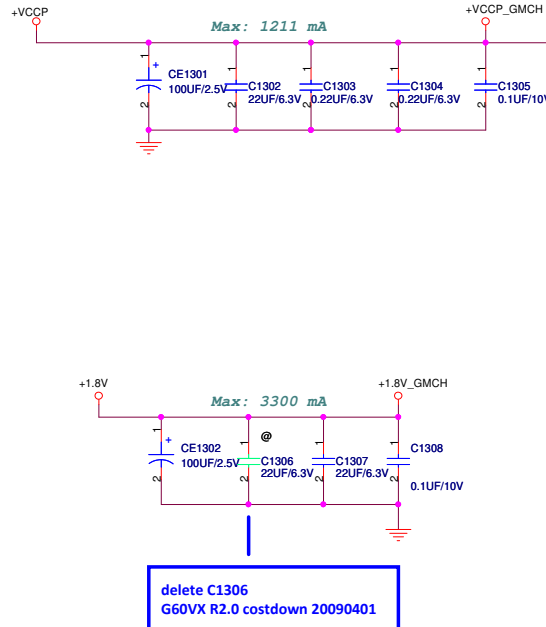
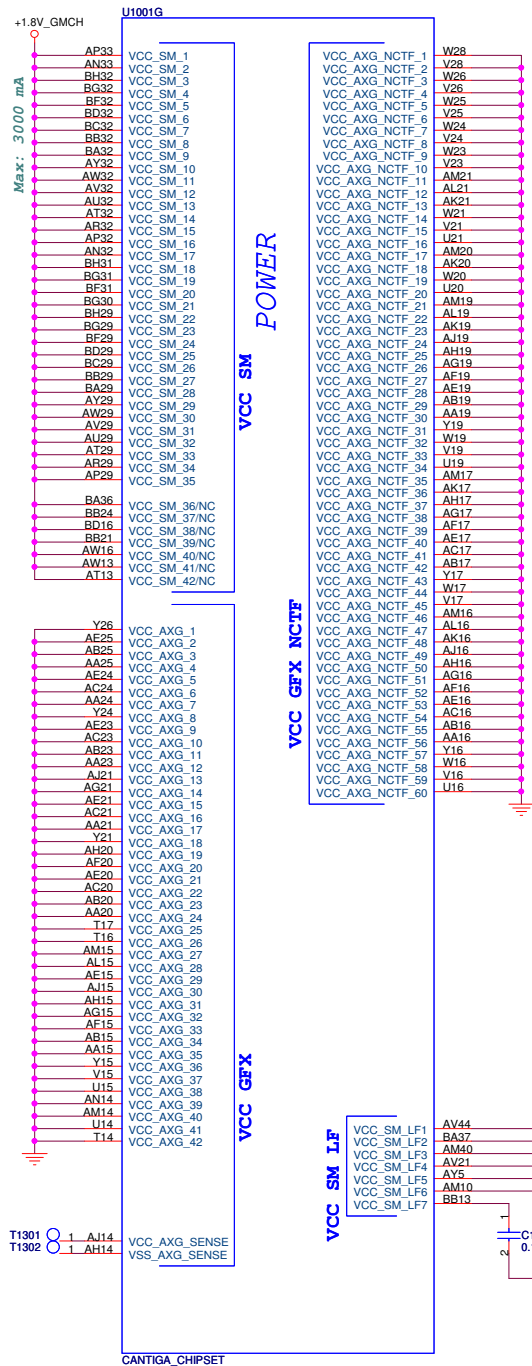
M_B_DM[0:7] 8

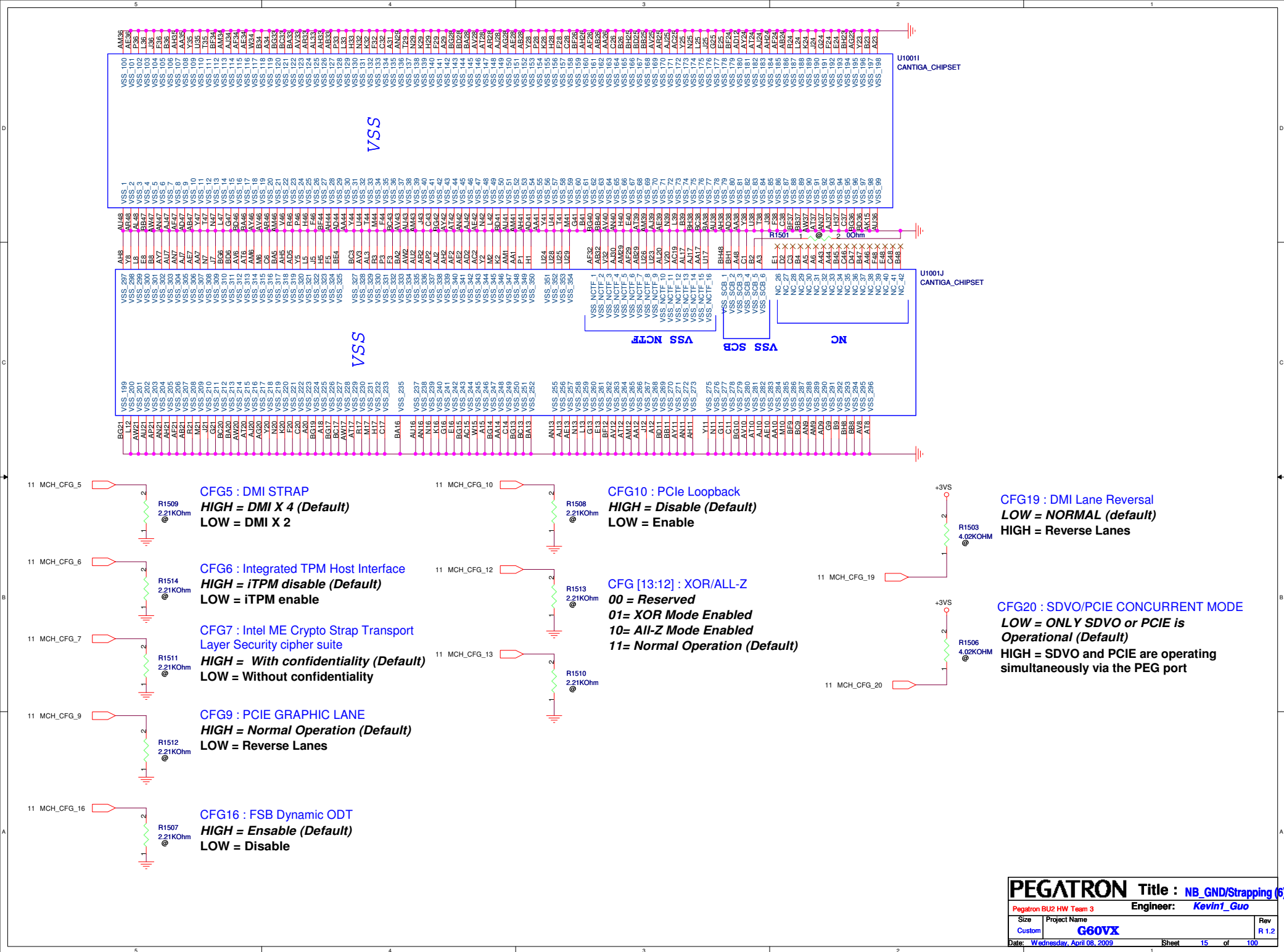
M_B_DQS[0:7] 8

M_B_DQS#[0:7] 8

M_B_A[0:14] 8.9

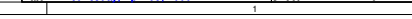
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Pegatron BU2 HW Team 3		Engineer: Kevin1_Guo	
Size	Project Name	Rev	
Custom	G60VX	R 1.2	
Date: Wednesday, April 08, 2009		Sheet	12 of 100

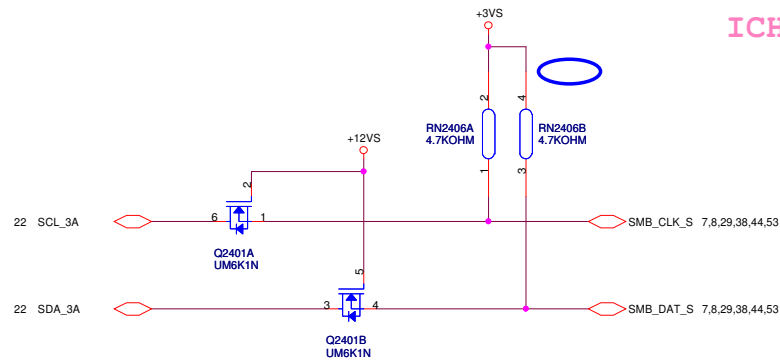




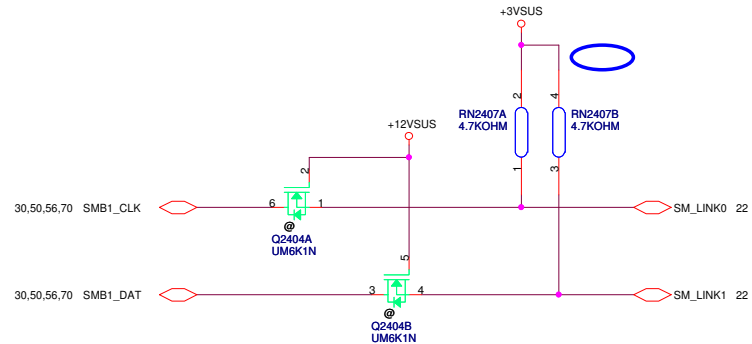
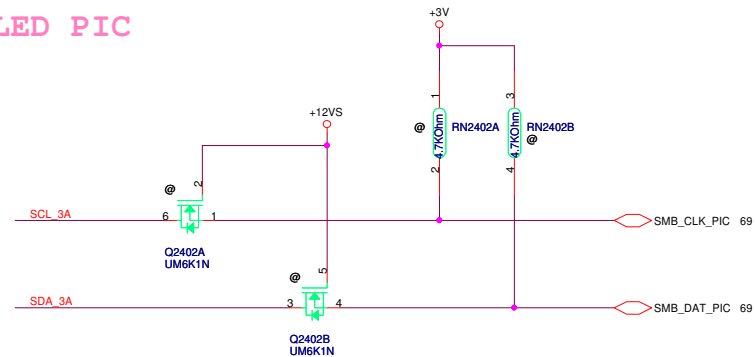
PEGATRON		Title : NB_****	
Pegatron BU2 HW Team 3		Engineer: Kevin1_Guo	
Size Custom	Project Name G60VX	Rev R 1.2	
Date: Thursday, March 05, 2009	Sheet	16	of 100

PEGATRON		Title : NB ****	
Pegatron BU2 HW Team 3		Engineer: Kevin1_Guo	
Size	Project Name		Rev
Custom	G60VX		R 1.2
Date: Thursday, March 05, 2009		Sheet	18 of 100





LED PIC



delete R2406 R2405; add RN2406
delete R2407 R2408; add RN2407
G60VX R2.0 costdown 20090401

PEGATRON		Title : SB_ICH9M-Other	
Pegatron BU2 HW Team 3		Engineer: Kevin1_Guo	
Size	Project Name	Rev	
Custom	G60VX	R 1.2	
Date: Thursday, April 02, 2009	Sheet 24 of 100		

PEGATRON		Title : SB ****	
Pegatron BU2 HW Team 3		Engineer: Kevin1_Guo	
Size	Project Name		Rev
Custom	G60VX		R 1.2
Date: Thursday, March 05, 2009		Sheet	26 of 100

PEGATRON		Title : SB ****	
Pegatron BU2 HW Team 3		Engineer: Kevin1_Guo	
Size	Project Name		Rev
Custom	G60VX		R 1.2
Date: Thursday, March 05, 2009		Sheet	28 of 100

unmount C2925,C2926 C2922
change R2901 to short land
G60VX R2.0 costdown 20090401

Latched Input Select

0 : Pin 17/18 = LCD_SSCG
1 : Pin 17/18 = PCIe_L0

0 : Pin 43/44 = SRC CLK
1 : Pin 43/44 = CPU_ITP CLK

0 : Pin 14/15 = PCIe_L9
Pin 17/18 = 27FIX/27SS
1 : Pin 14/15 = DOT_96MHz
Pin 17/18 = LCD_SSCG/PCIe_L0

0 : Pin 40/41 = PCIe_L7
1 : Pin 40/41 = PEREQ#

PEREQ1#:

PEREQ1# R2922 1 2 10KOhm

PEREQ2#:

PEREQ2# R2923 1 2 10KOhm

PEREQ3# : PCIeX2/4

PEREQ4# : PCIeX3/5/7

These two pins
need to be
latched in to
select the source
of PCICLKs:
high = SATA PLL
low = PCIeX PLL

For 364 Over-clocking

33PC11 R2932 1 2 10KOhm

R2929 1 2 10KOhm

REF0 R2931 1 2 10KOhm

R2930 1 2 10KOhm

R1.2

Reserved for R1.0 Debug

BCLK	FSB	BSEL2	BSEL1	BSEL0
166	667	0	1	1
200	800	0	1	0
266	1067	0	0	0

Pegatron Title : CLK_ICS9LPR363

Pegatron BU2 HW Team 3

Engineer: Kevin1_Guo

Size

Custom

Project Name

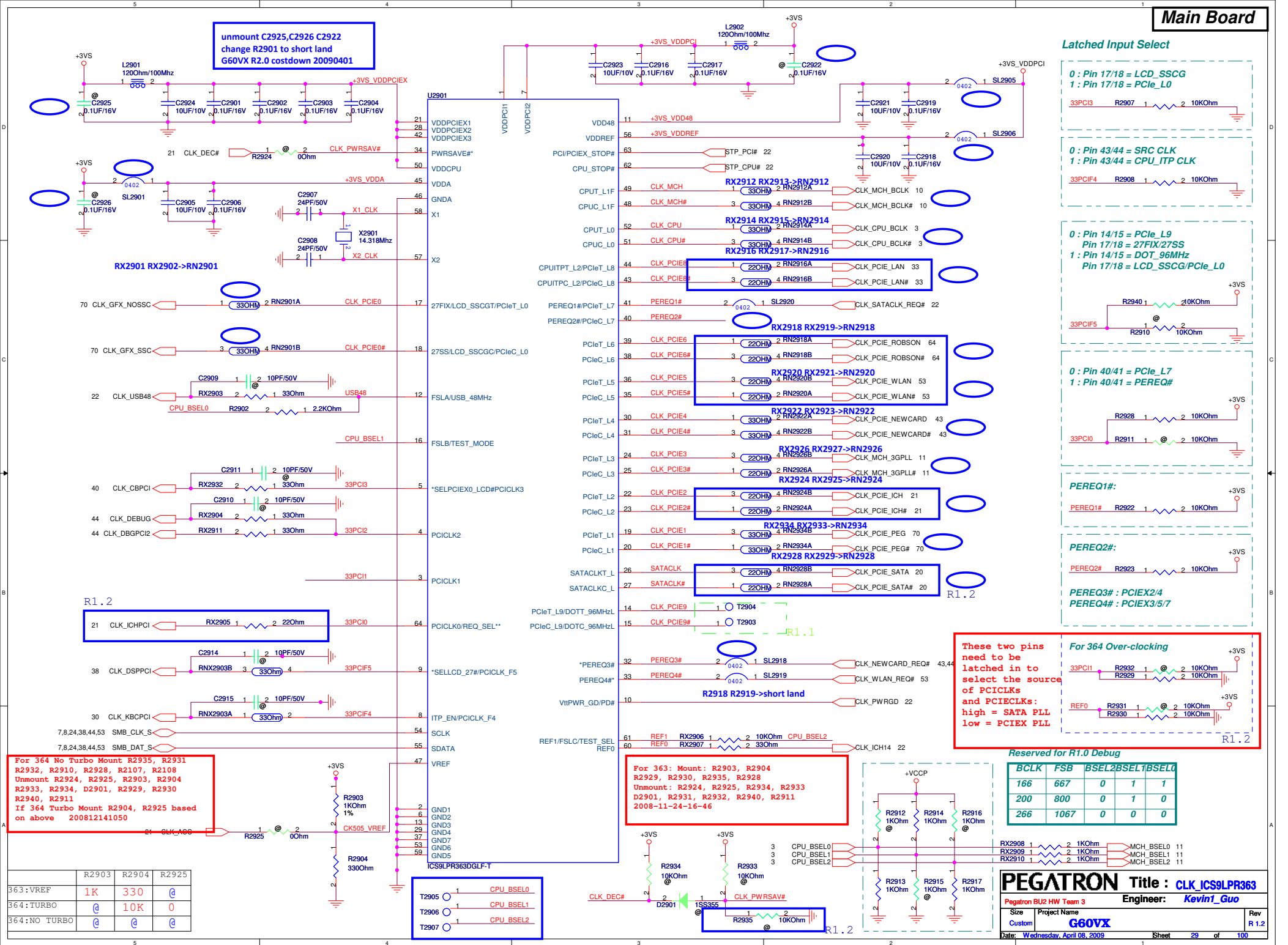
G60VX

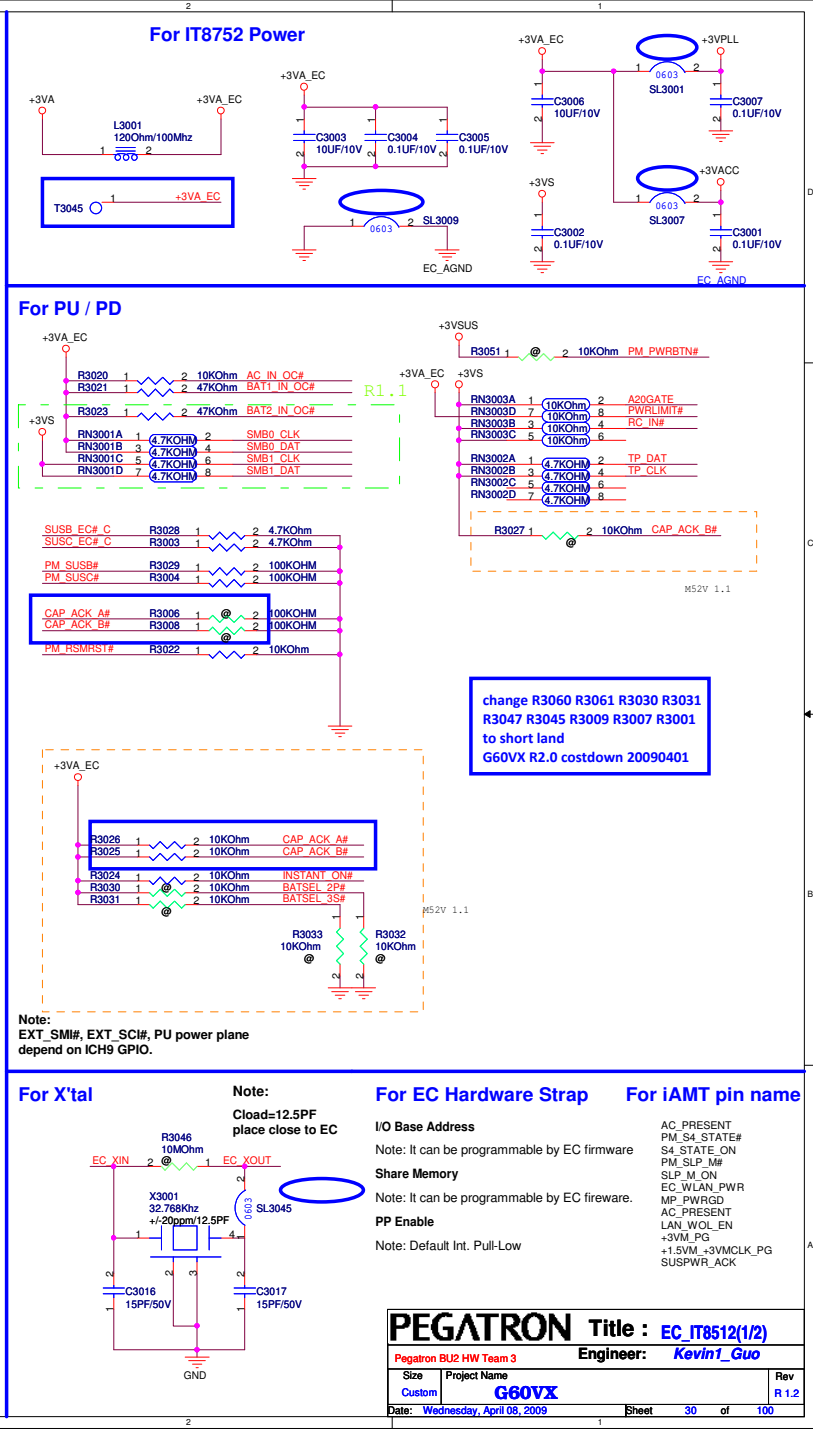
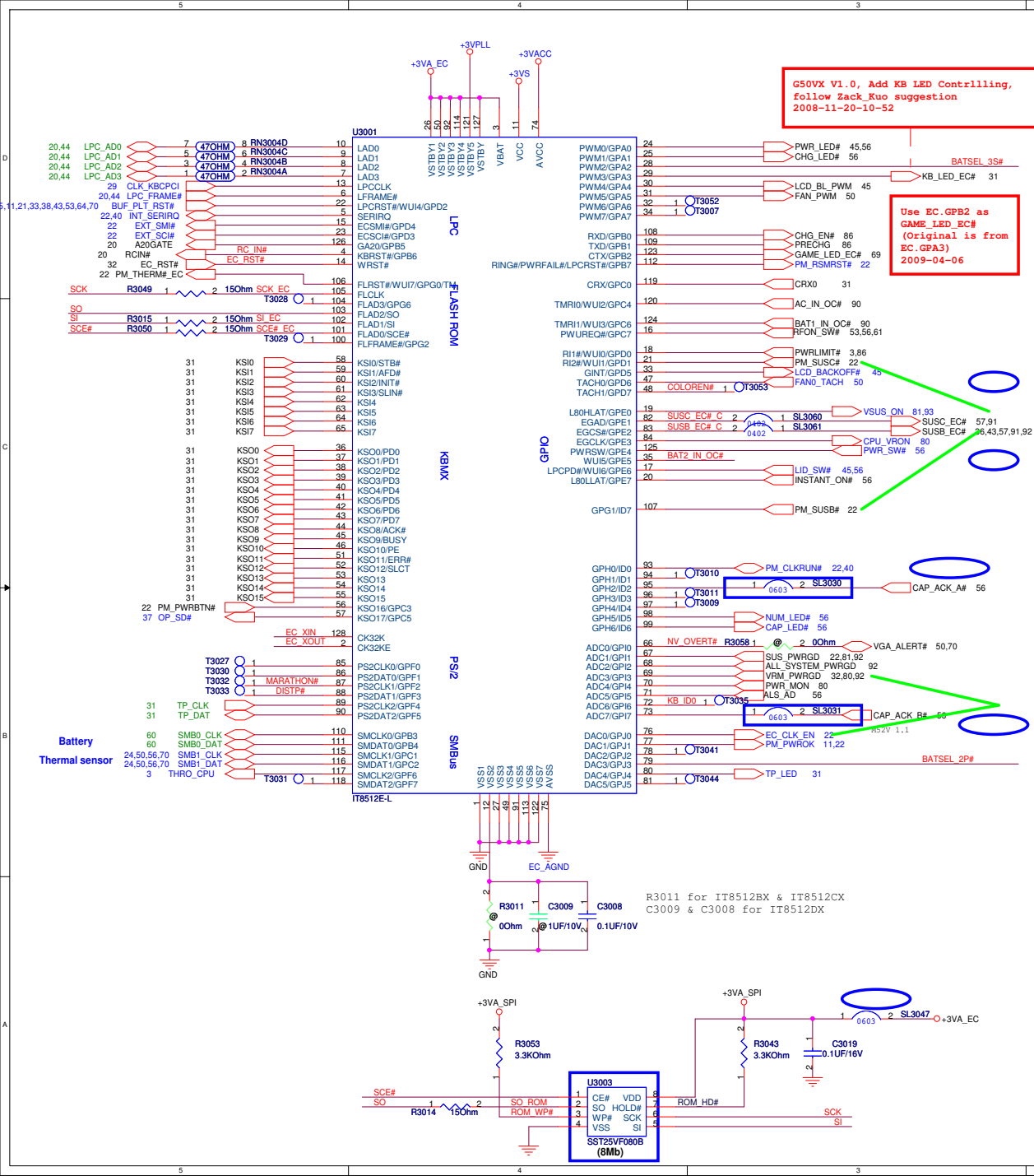
Date: Wednesday, April 08, 2009

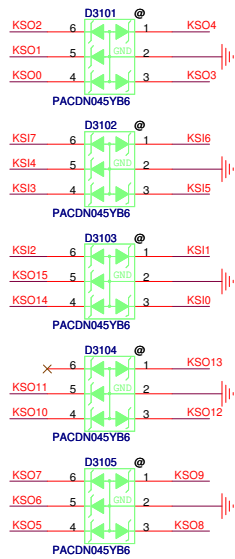
Sheet 29 of 100

Rev

R1.2

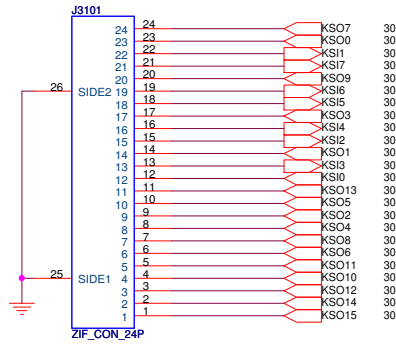
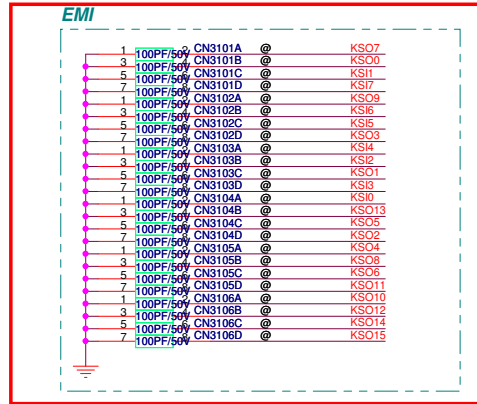






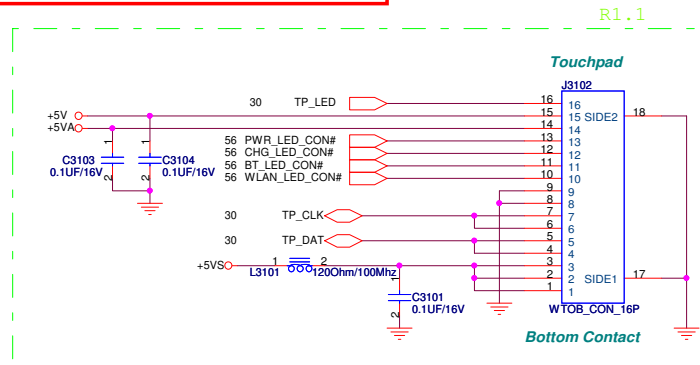
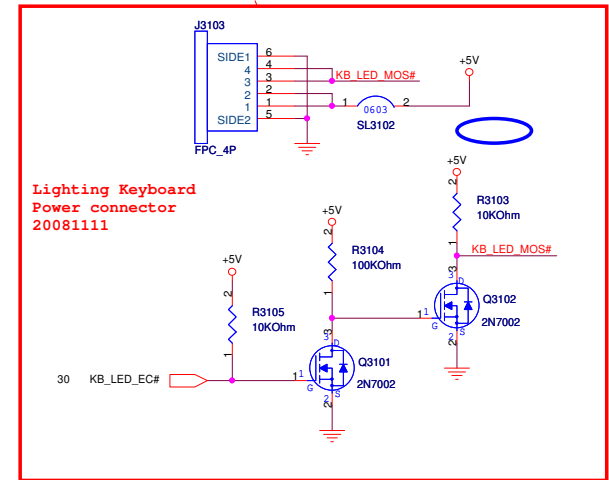
G50VX R1.1 Change back
20090113

Keyboard

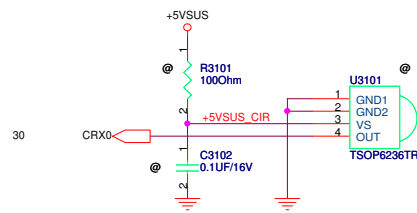


FPC_4P Reference P/N
12G183100402

change R3102 to 0603 short land
G60VX R2.0 costdown 20090401

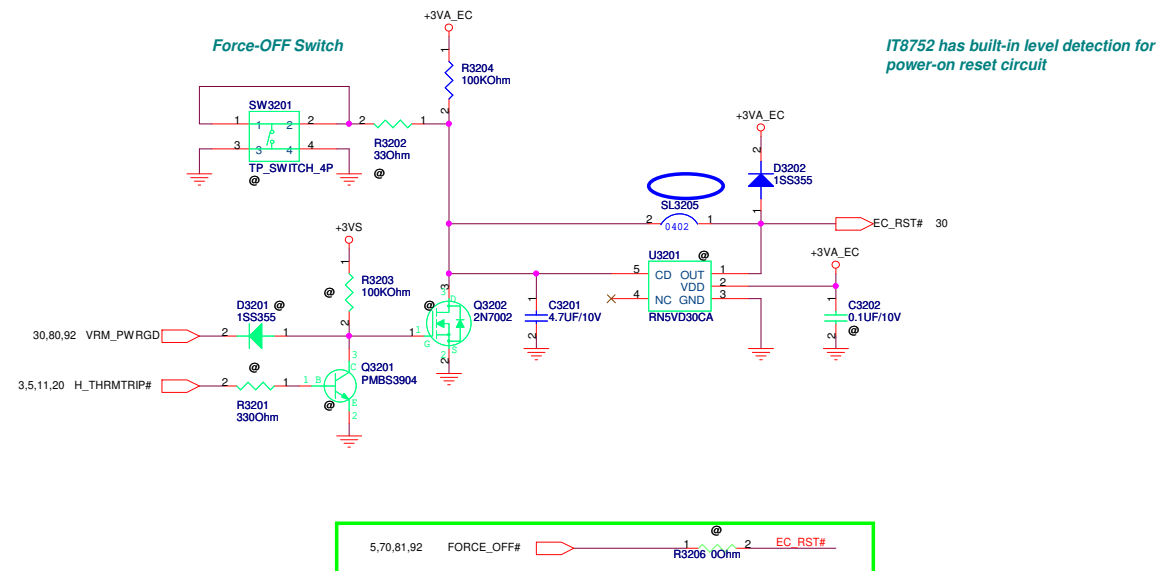


CIR

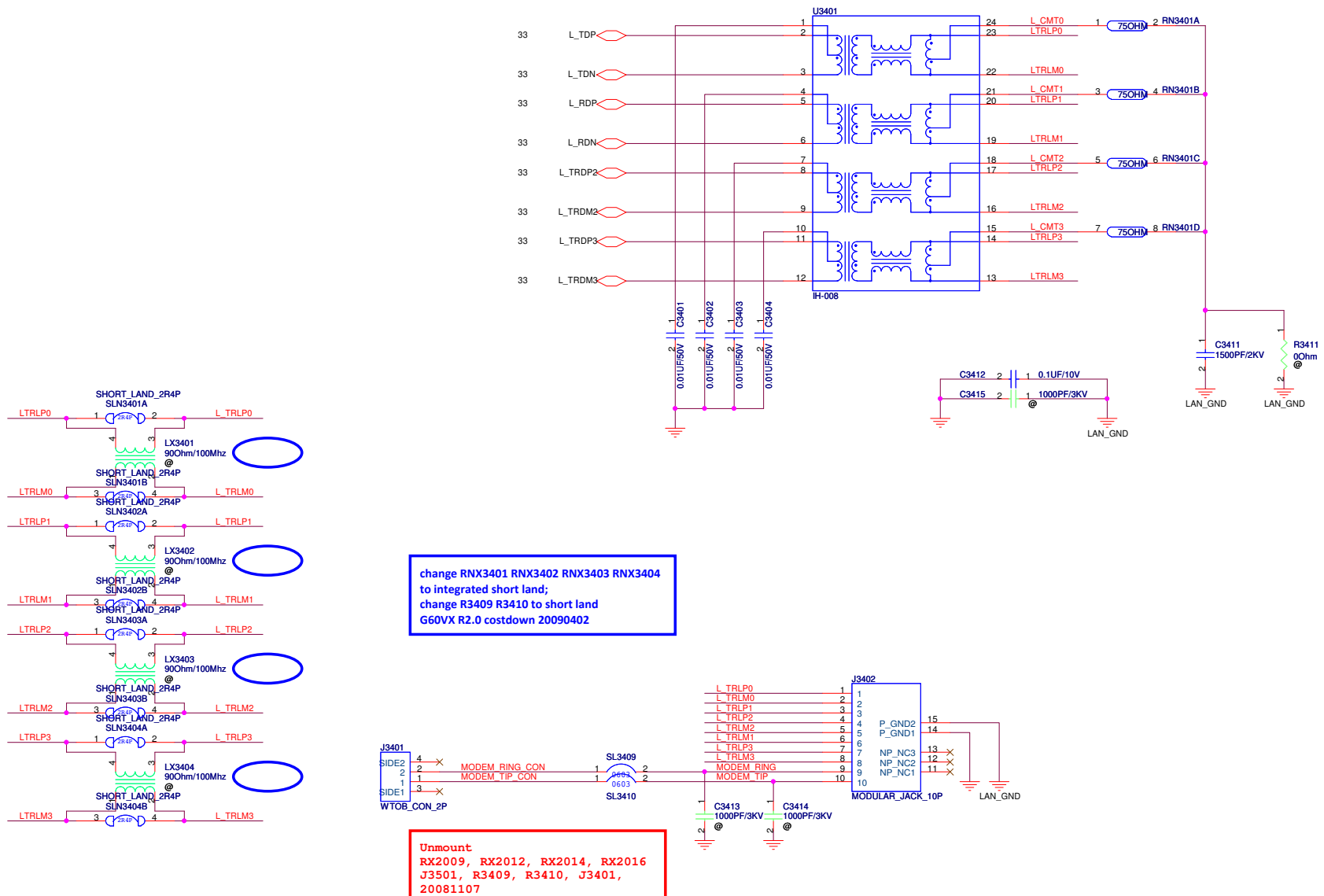


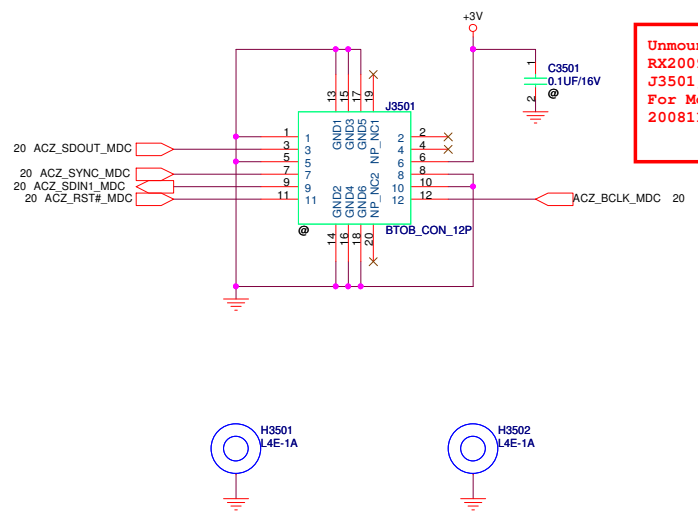
Unmount U3101
R3101, C3102 For
delete CIR
20081107

unmount SW3201 D3201 R3201 R3202 R3203 Q3201 Q3202
change R3205 to short land
G60VX R2.0 costdown 20090401



Reserve this part for protection
G60VX R1.2 20090305

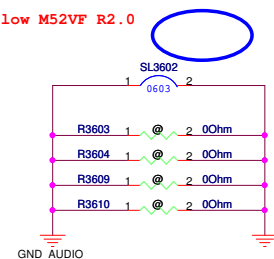
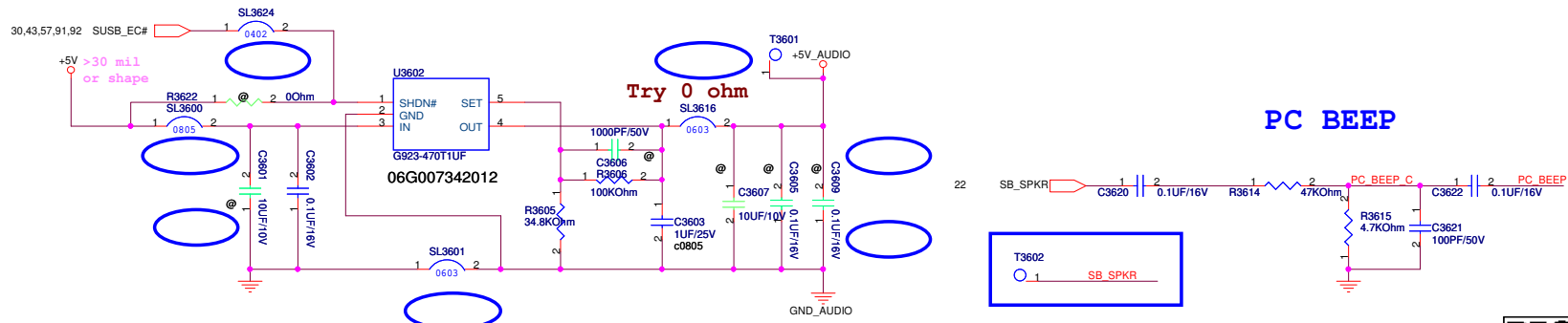
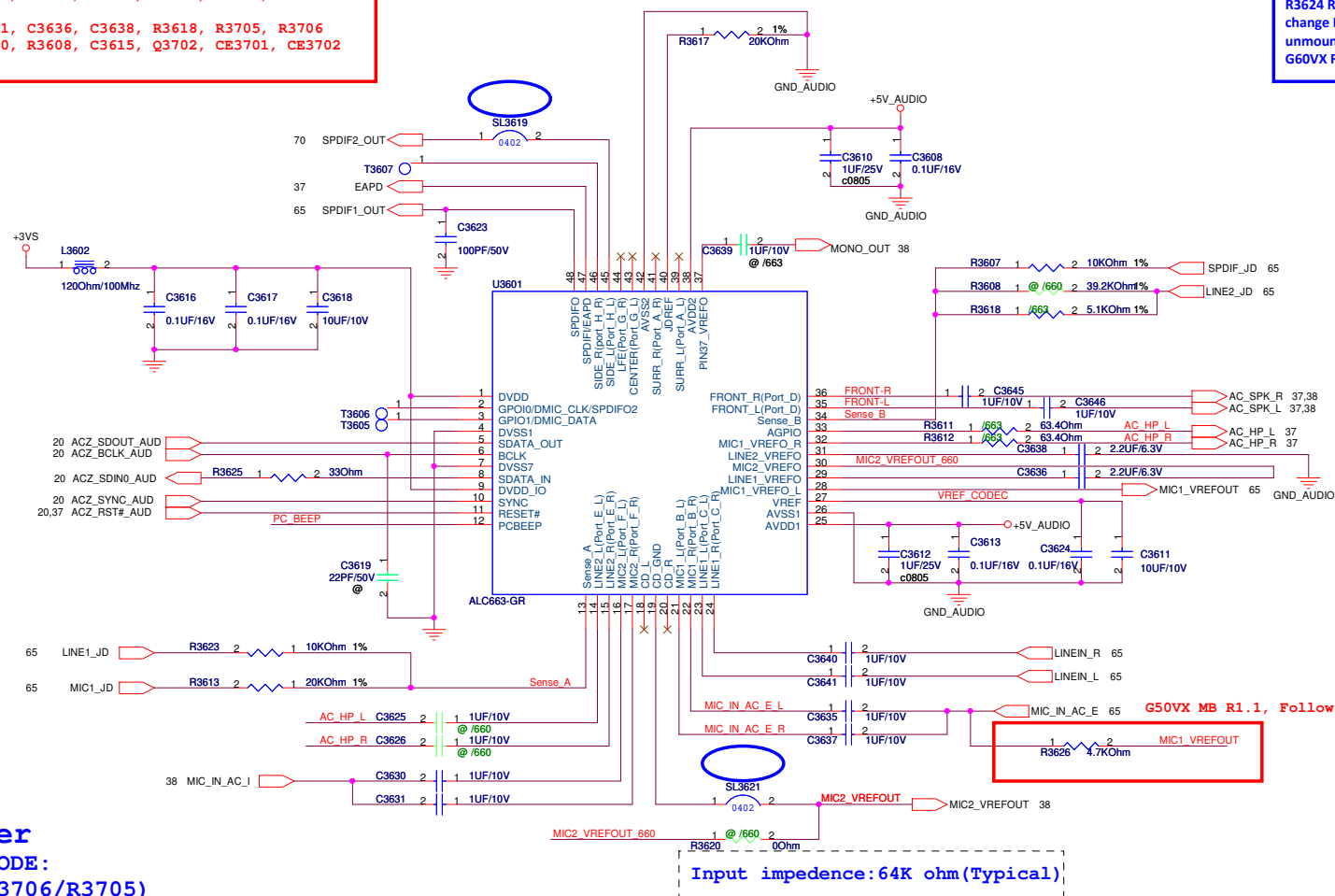




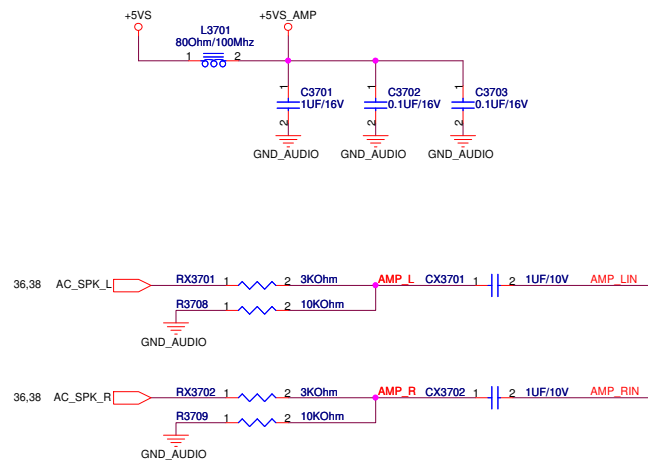
Unmount
RX2009, RX2012, RX2014, RX2016
J3501, R3409, R3410, J3401,
For Modem Delete
20081107

If ALC662LJ
Mount LJ C3625, C3626, R3620, R3608, C3615, Q3702, CE3701, CE3702
Unmount LJ R3611, R3612, R3621, C3636, C3638, R3618, R3705, R3706
If ALC663LJ
Mount LJ R3611, R3612, R3621, C3636, C3638, R3618, R3705, R3706
Unmount LJ C3625, C3626, R3620, R3608, C3615, Q3702, CE3701, CE3702

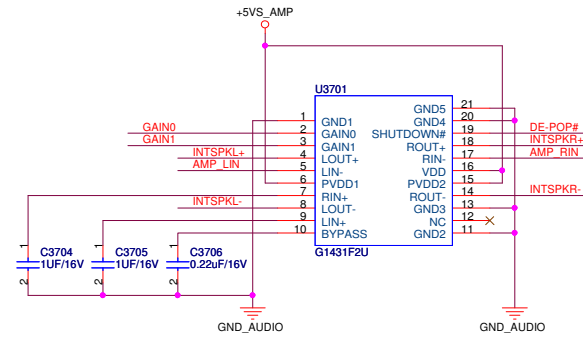
change R3619 R3621 R3602
R3624 R3601 R3616 to short land;
change L3601 to short land;
unmount C3601 C3605 C3609;
G60VX R2.0 costdown 20090402



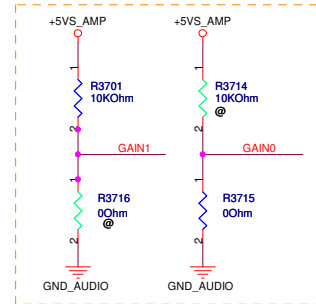
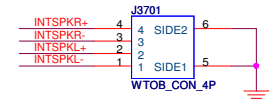
PEGATRON		Title : CODEC-ALC663	
Pegatron BU2 HW Team 3		Engineer: Kevin1_Guo	
Size	Project Name		
Custom	G60VX		
Date: Wednesday, April 08, 2009	Sheet	36	of 100
		Rev	R 1.2



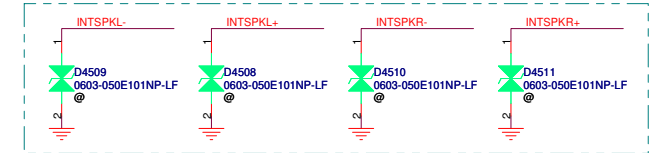
GAIN0	GAIN1	Av (inv)
0	0	6 dB
0	1	10 dB
1	0	15.6 dB
1	1	21.6 dB



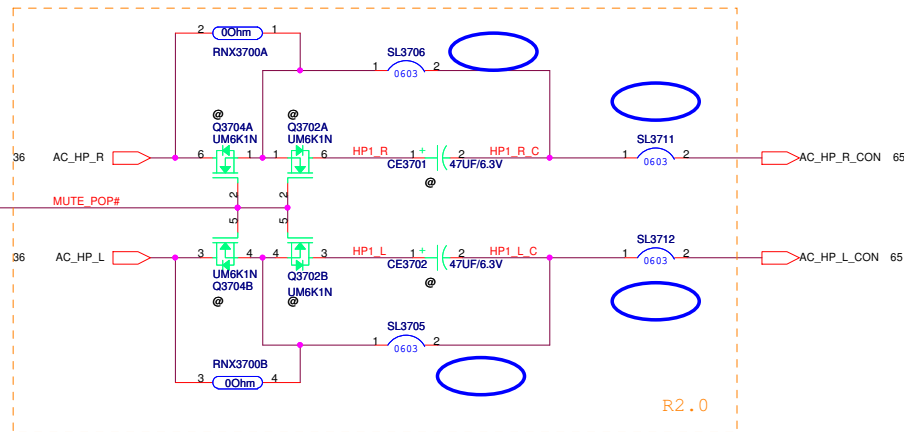
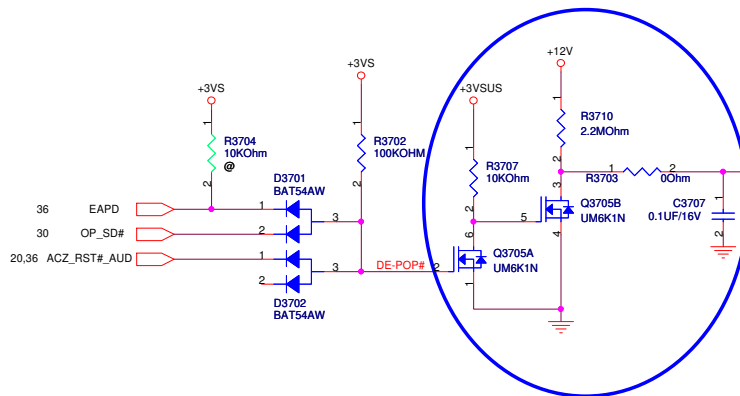
Internal Speaker Conn.



Reserved for EMI

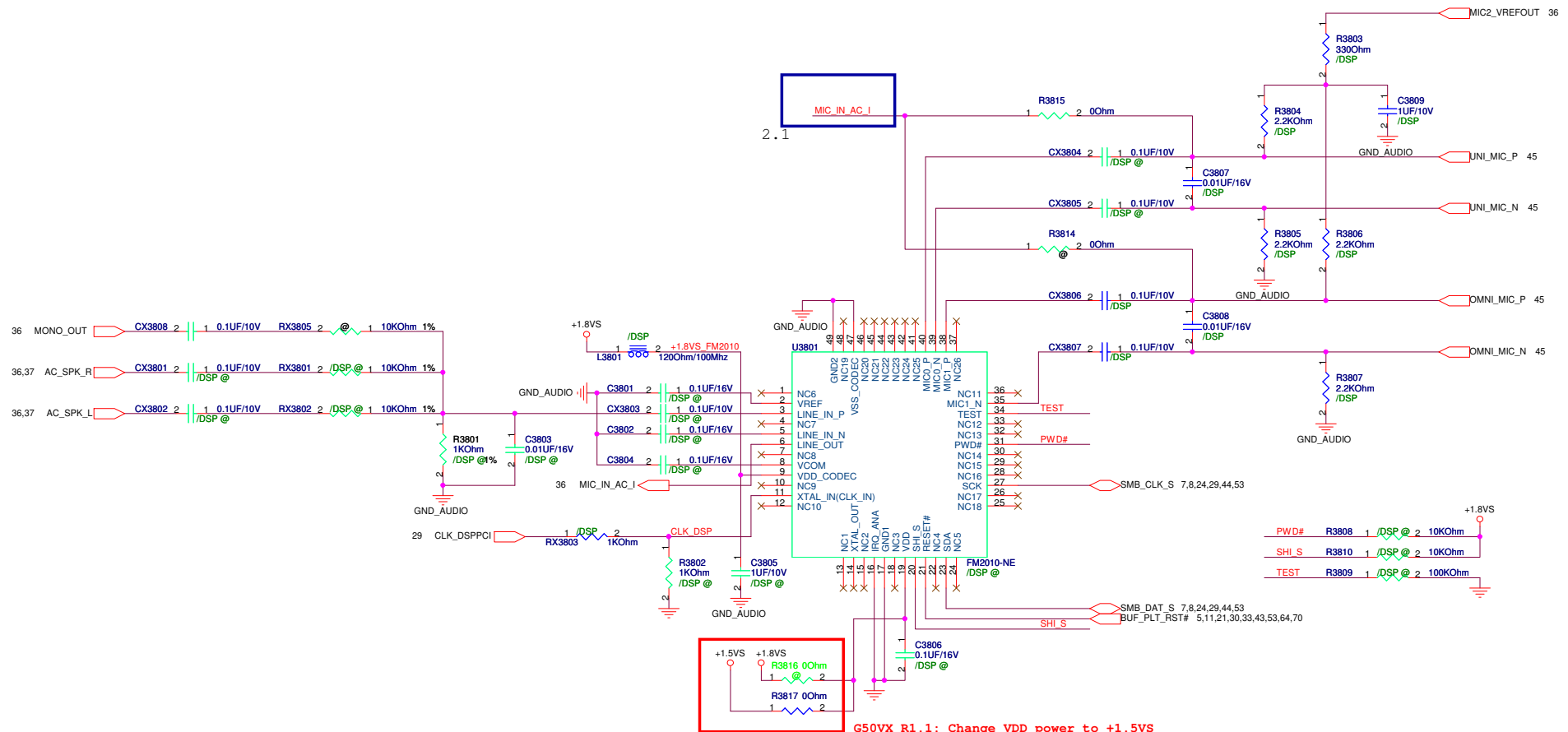


R2.0



R2.0

unmount R3707 Q3705 R3710 R3703 C3707
change R3706 R3705 R3711 R3712 to short land
add SL3700 SL3701
G60VX R2.0 costdown 20090402

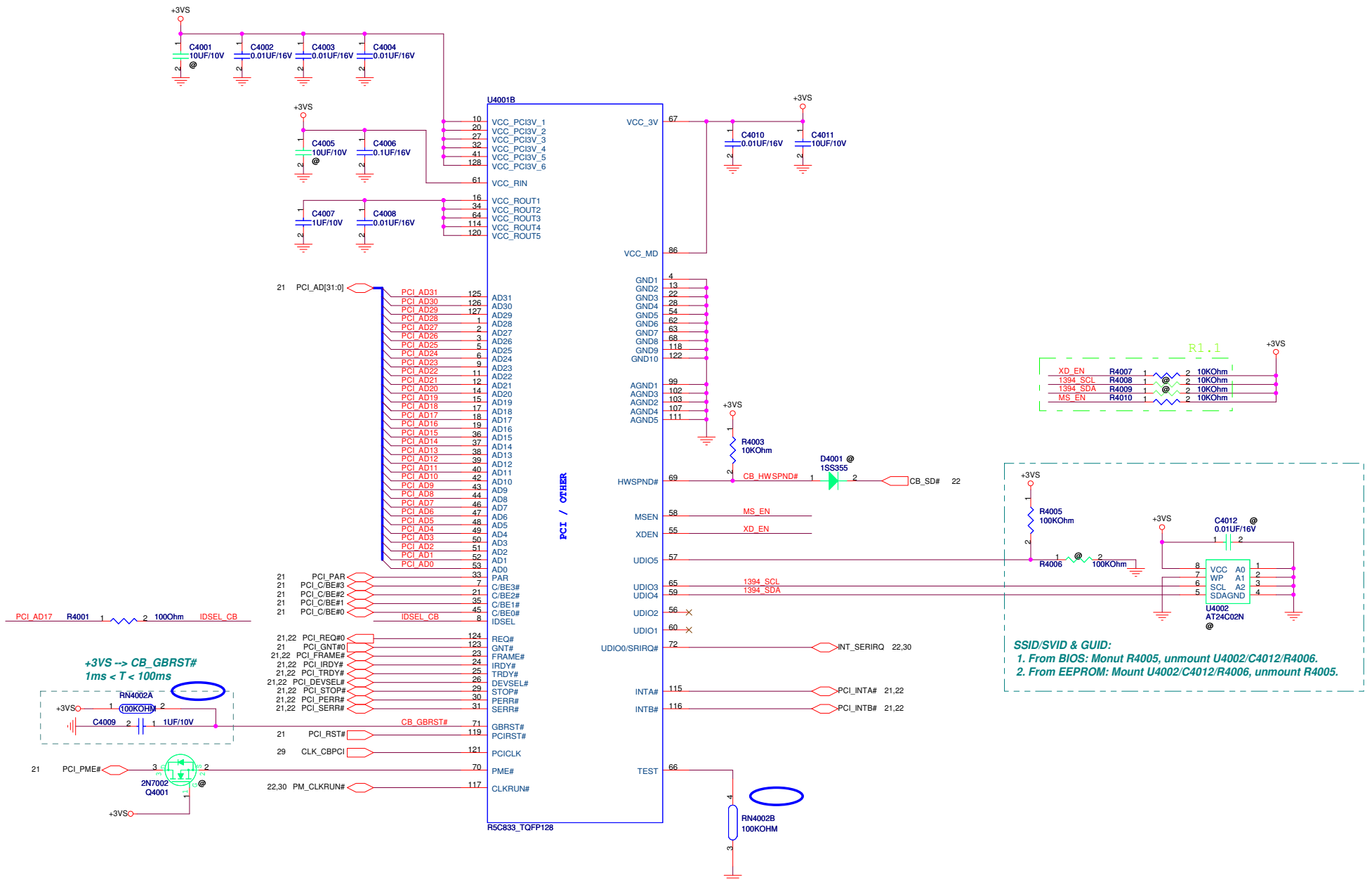


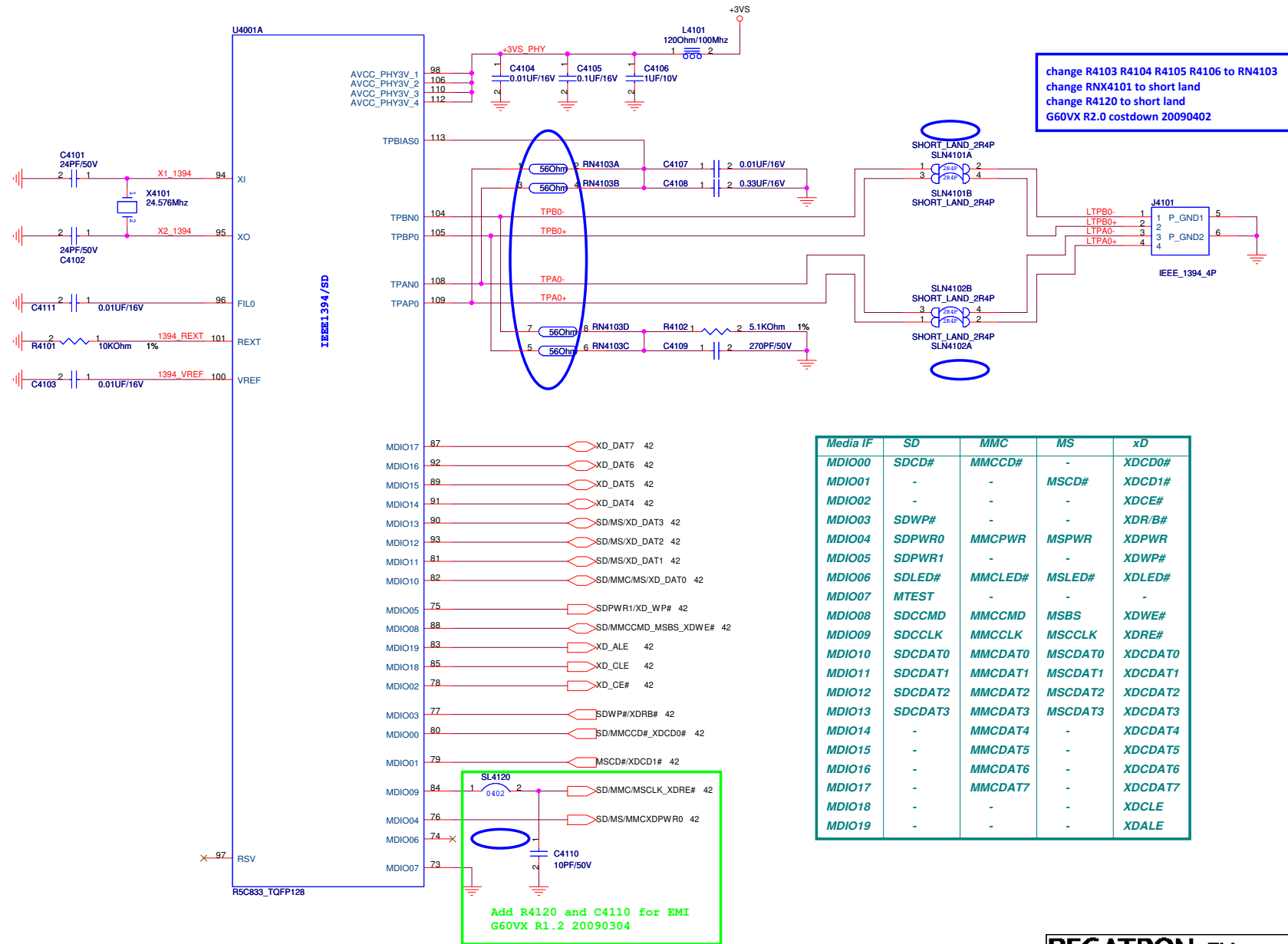
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Mount R4507, R508, R4509, R4510
U3801, R3803, C3809, R3804, CX3804, C3807, CX3805,
R3805, CX3806, CX3806, CX3807, C3808, R3807
R3808, R3810, R3809, C3806, C3805, R3802, RX3803
C3804, C3802, CX3803, C3801, L3801, C3803, R3801
RX3801, RX3802, CX3801, CX3802

Unmount R3815, R3814, CX3808, RX3805
For supporting Array Mic
20081107
```

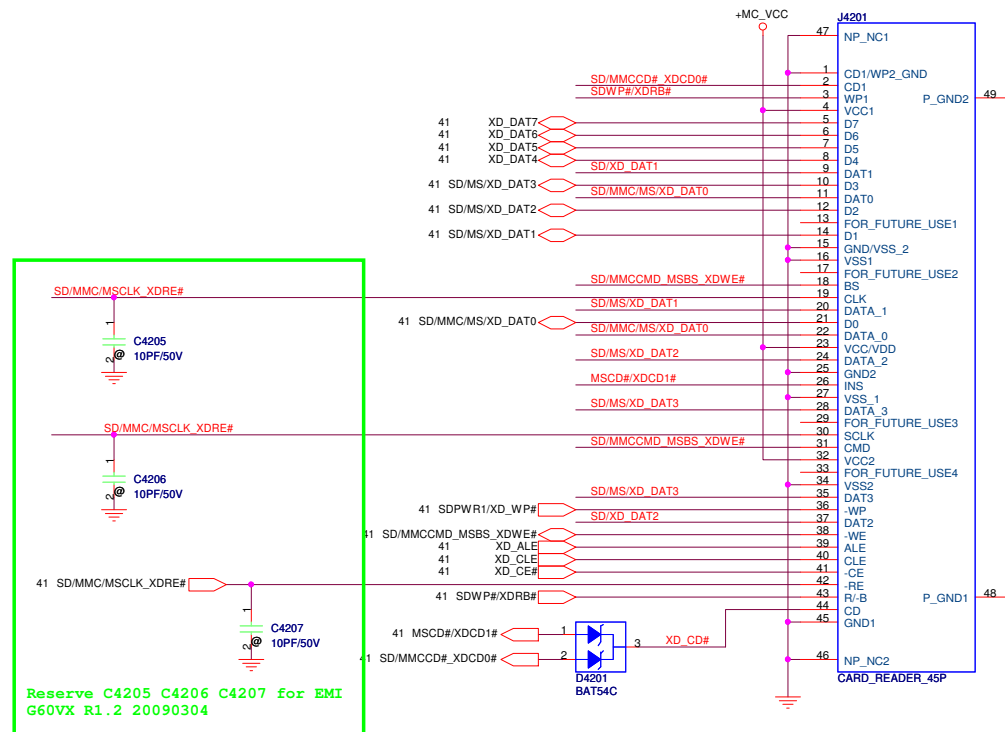
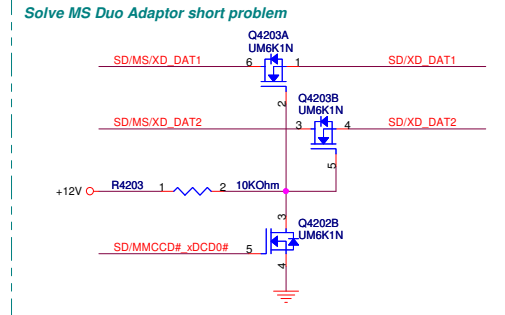
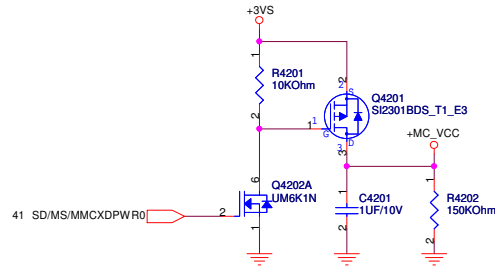
G50VX R1.1: Change VDD power to +1.5VS to decrease the digital noise and for less power consumption

PEGATRON		Title : <u>AUD_FM2010</u>	
Pegatron BU2 HW Team 3		Engineer: <u>Kevin1_Guo</u>	
Size Custom	Project Name G60VX	Rev R 1.2	
Date: <u>Wednesday, April 08, 2009</u>	Sheet	38	of 100

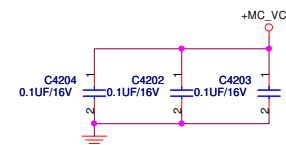




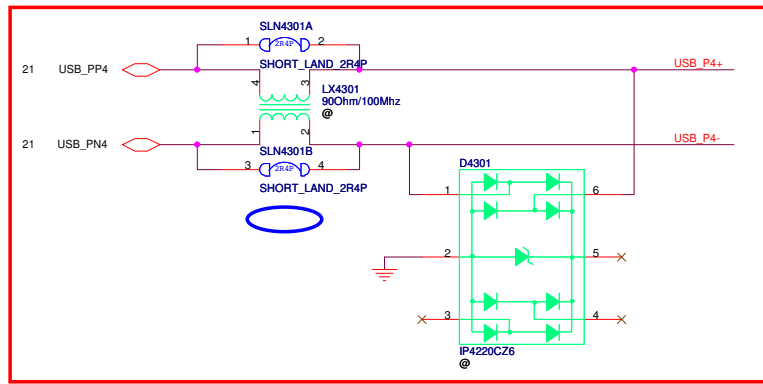
Media IF	SD	MMC	MS	xD
MDIO00	SDCD#	MMCCD#	-	XDCD0#
MDIO01	-	-	MSCD#	XDCD1#
MDIO02	-	-	-	XDCE#
MDIO03	SDWP#	-	-	XDR/B#
MDIO04	SDPWR0	MMCPWR	MSPWR	XDPR
MDIO05	SDPWR1	-	-	XDWP#
MDIO06	SDLED#	MMCLEd#	MSLED#	XDLED#
MDIO07	MTEST	-	-	-
MDIO08	SDCCMD	MMCCMD	MSBS	XDWE#
MDIO09	SDCCLK	MMCCCLK	MSCCLK	XDRE#
MDIO10	SDCDAT0	MMCDAT0	MSCDAT0	XDCDAT0
MDIO11	SDCDAT1	MMCDAT1	MSCDAT1	XDCDAT1
MDIO12	SDCDAT2	MMCDAT2	MSCDAT2	XDCDAT2
MDIO13	SDCDAT3	MMCDAT3	MSCDAT3	XDCDAT3
MDIO14	-	MMCDAT4	-	XDCDAT4
MDIO15	-	MMCDAT5	-	XDCDAT5
MDIO16	-	MMCDAT6	-	XDCDAT6
MDIO17	-	MMCDAT7	-	XDCDAT7
MDIO18	-	-	-	XDCLC
MDIO19	-	-	-	XDALE



Reserve C4205 C4206 C4207 for EMI
G60VX R1.2 20090304

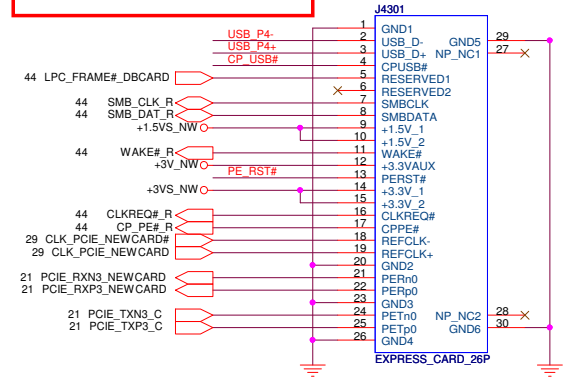


PEGATRON		Title : CB 4in1 CardReader	
Pegatron BU2 HW Team 3		Engineer: Kevin1_Guo	
Size	Project Name	Rev	
Custom	G60VX	R 1.2	
Date: Wednesday, April 08, 2009	Sheet	42	of 100

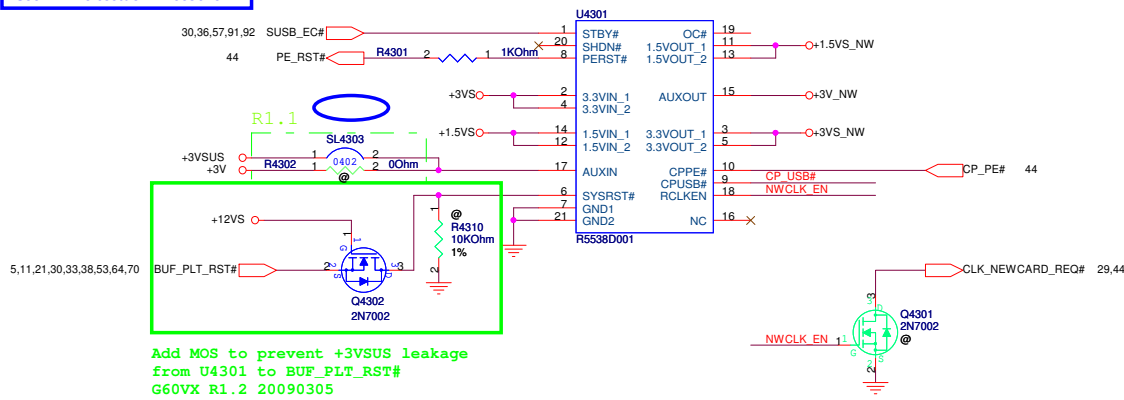


Change Newcard to USB port 4
G50VX R1.1 20090108

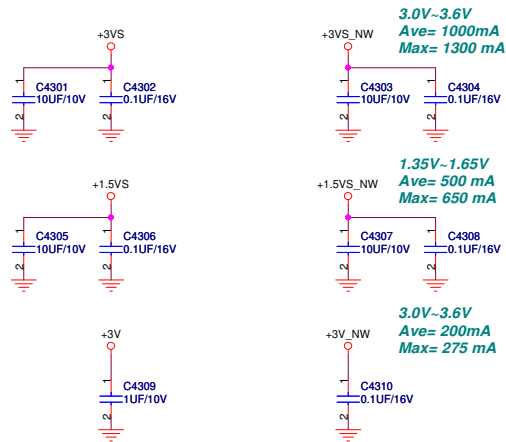
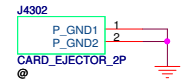
NewCard Header



change RN4301 to short land
change R4303 to short land
G60VX R2.0 costdown 20090402

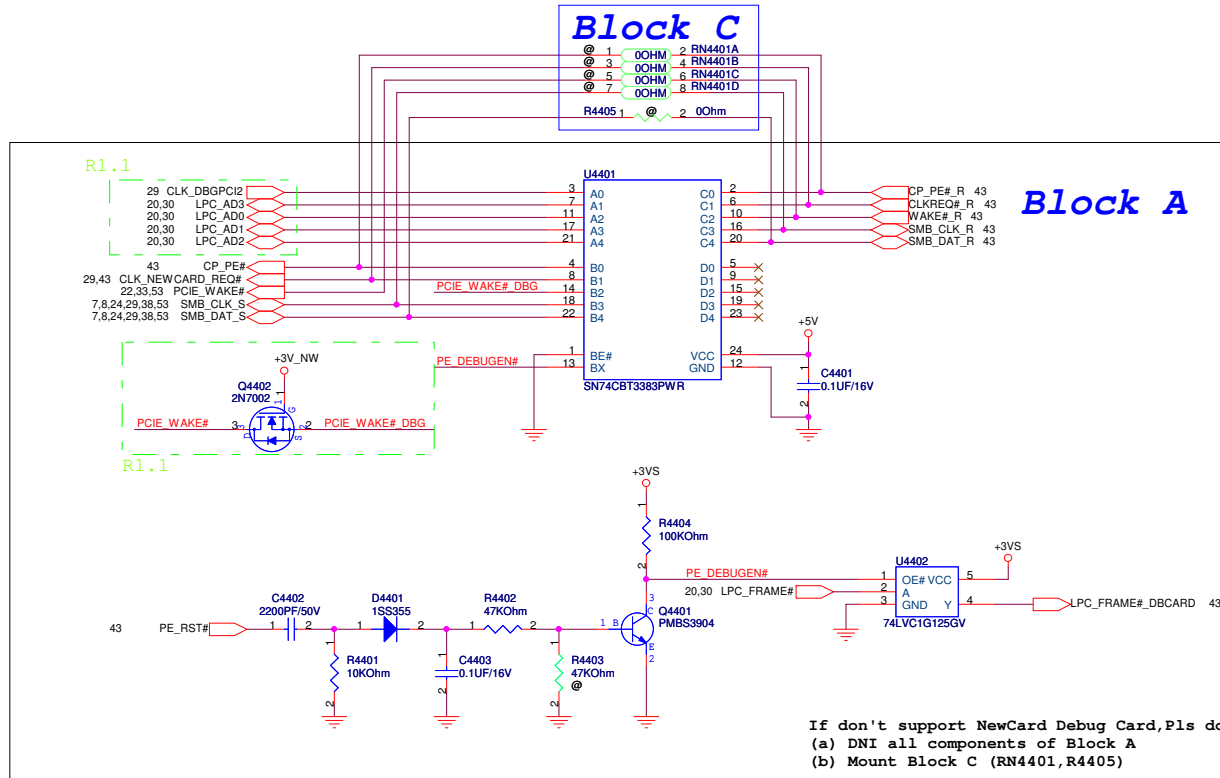


NewCard Ejector

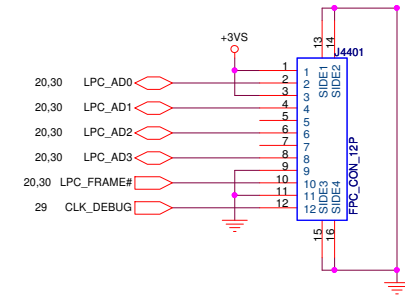


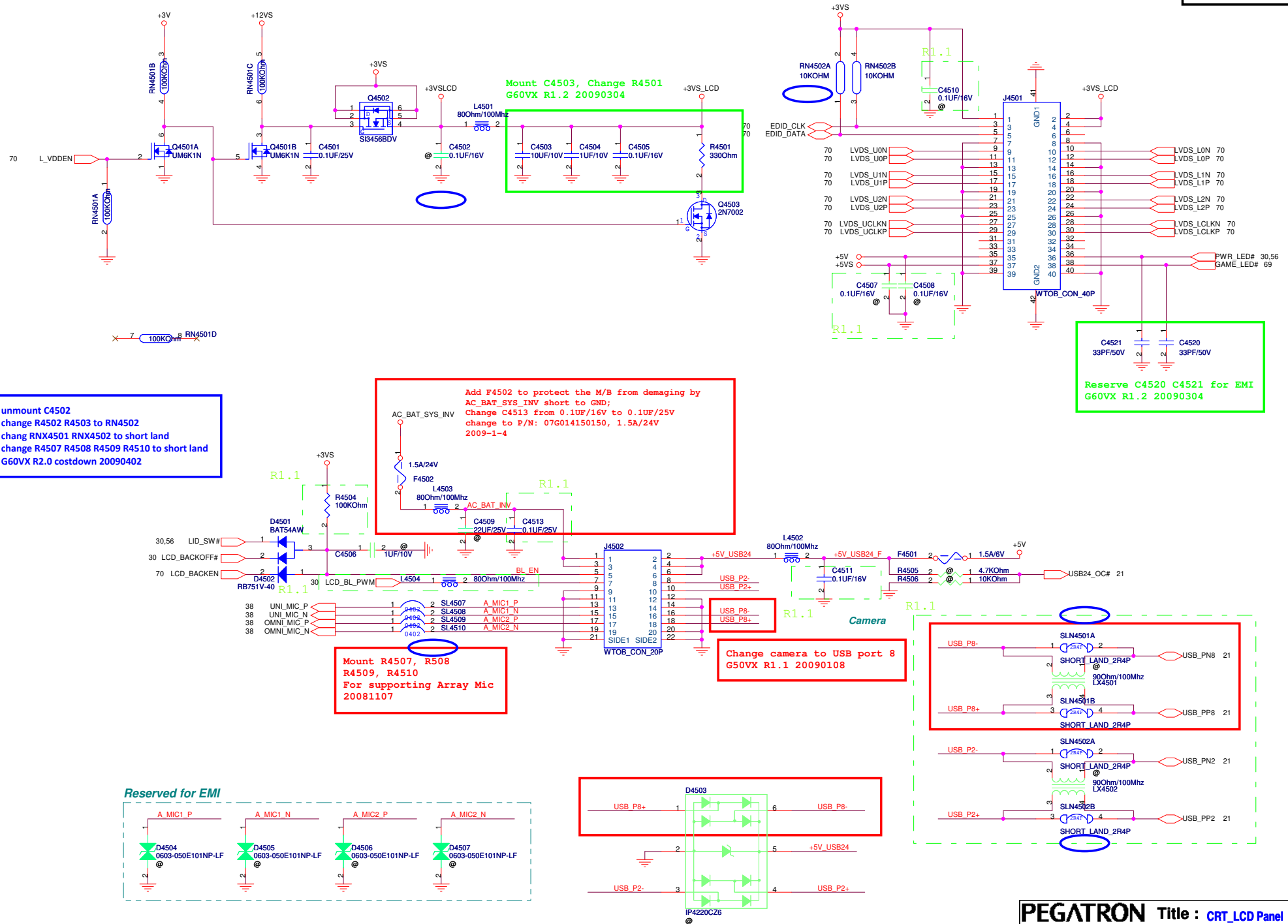
For NewCard Debug Card

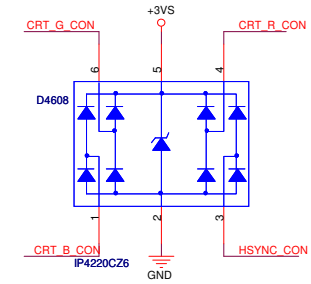
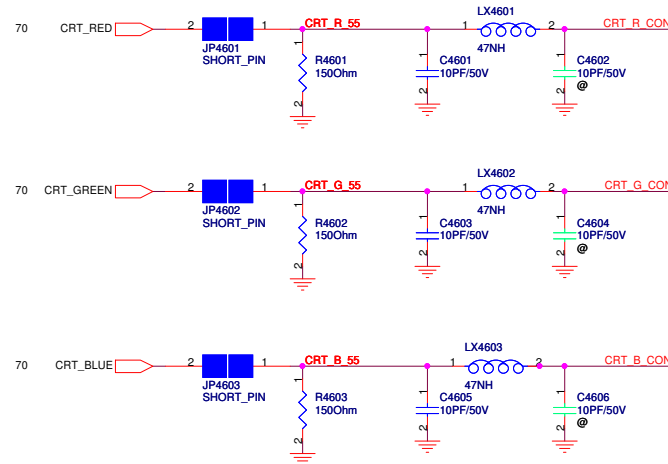
LPC Debug Port



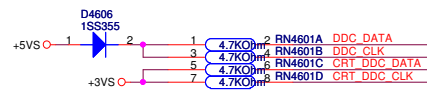
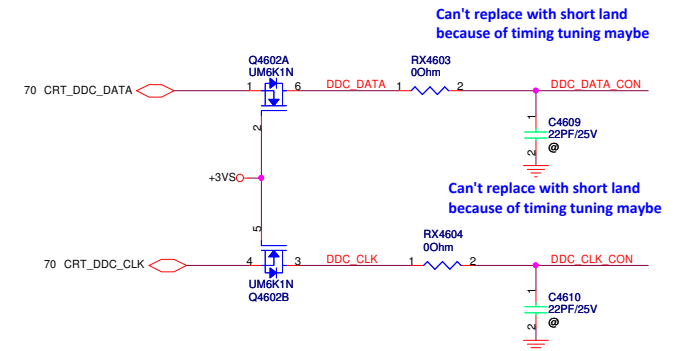
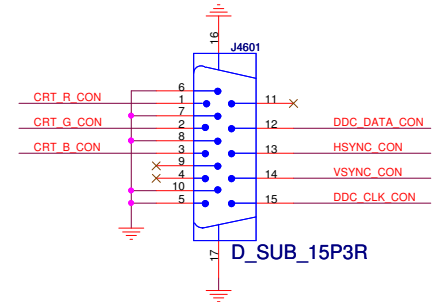
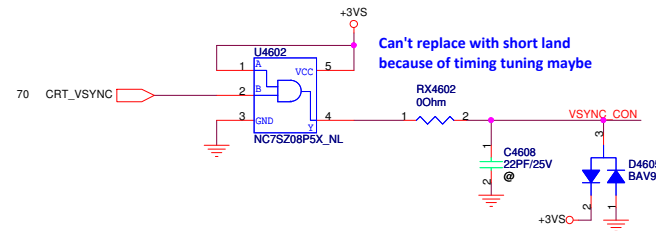
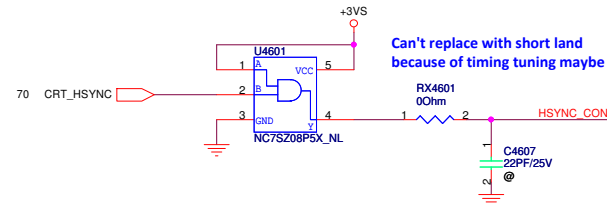
Mount Block A and LPC Debug Port in early stage
200811170917



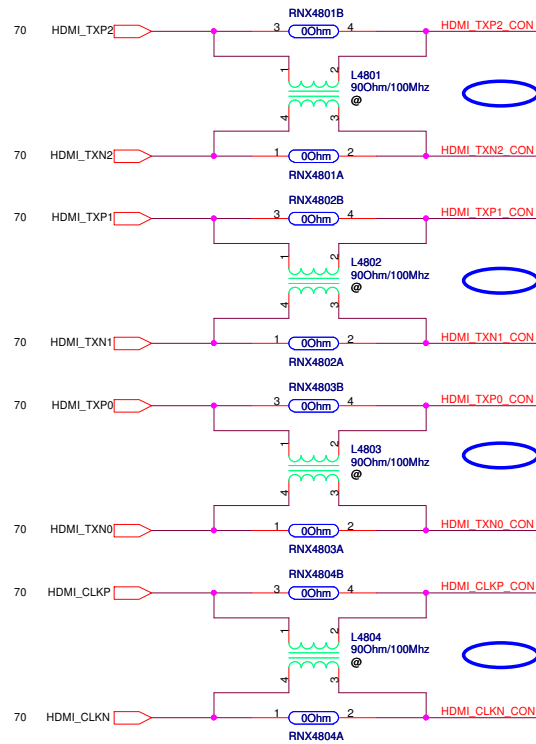




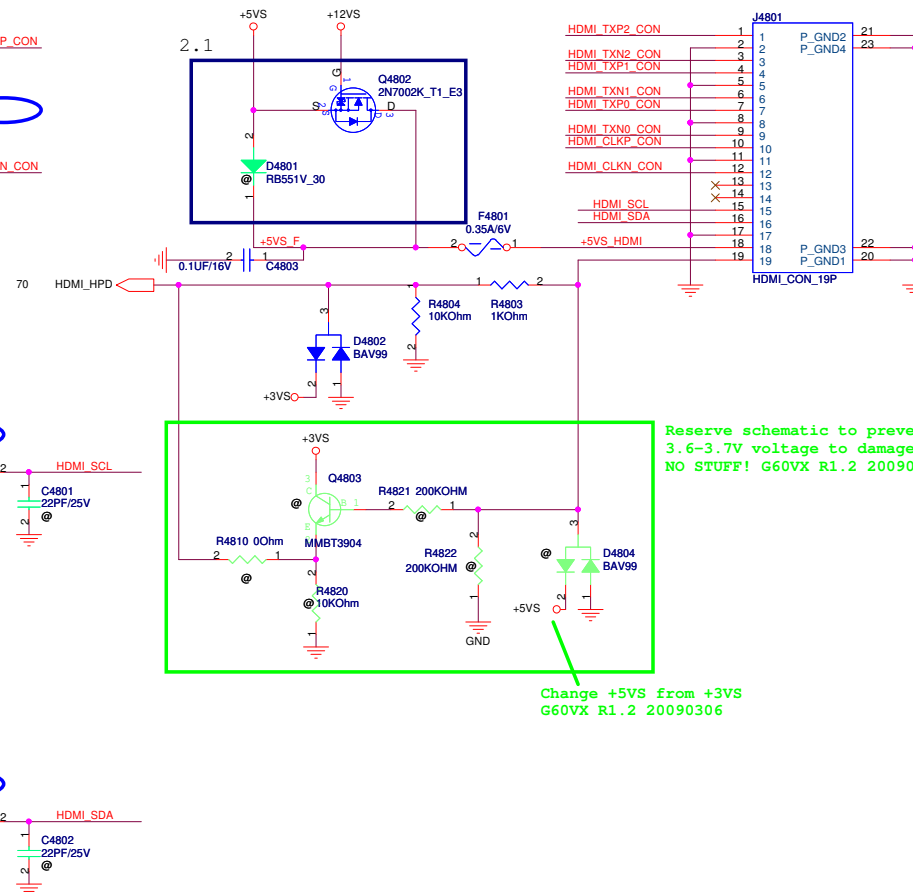
delete RX4605 RX4606 RX4607
delete D4601 D4602 D4603 D4604
add D4608
change RN4601 to 4R8P
delete RN4602
G60VX R2.0 costdown 20090402



PEGATRON		Title : CRT D-Sub	
Pegatron BU2 HW Team 3		Engineer: Kevin1_Guo	
Size	Project Name	Rev	
Custom	G60VX	R 1.2	
Date: Thursday, April 02, 2009	Sheet	46	of 100



Reserve RNX4801 RNX4802 RNX4803 RNX4804
delete RX4809 RX4810 / use short land;
delete R4801 R4802 / add RN4801
G60VX R2.0 costdown 20090402



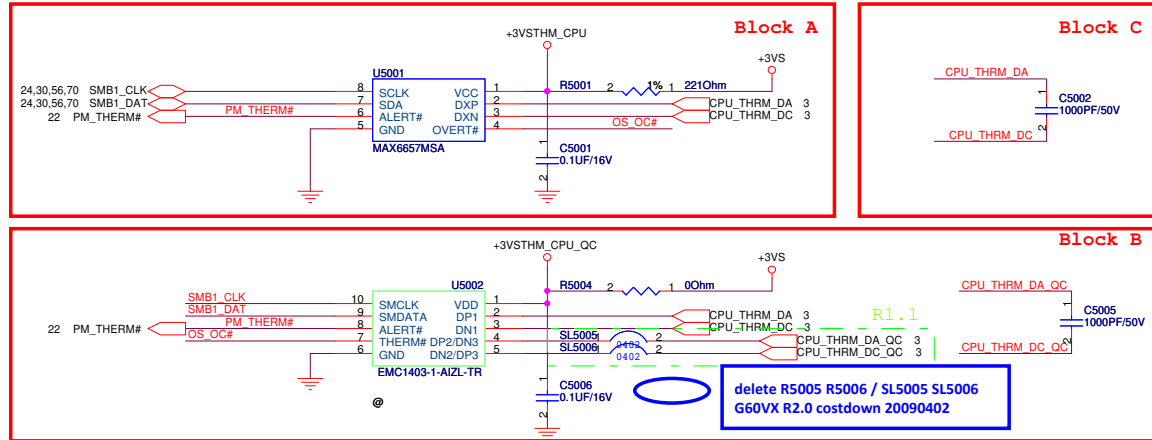
Reserve schematic to prevent the
3.6-3.7V voltage to damage the GPU
NO STUFF! G60VX R1.2 20090304

Change +5VS from +3VS
G60VX R1.2 20090306

PEGATRON		Title : TV HDMI	
Pegatron BU2 HW Team 3		Engineer: Kevin1_Guo	
Size	Project Name	Rev	
Custom	G60VX	R 1.2	
Date: Wednesday, April 08, 2009	Sheet	48	of 100

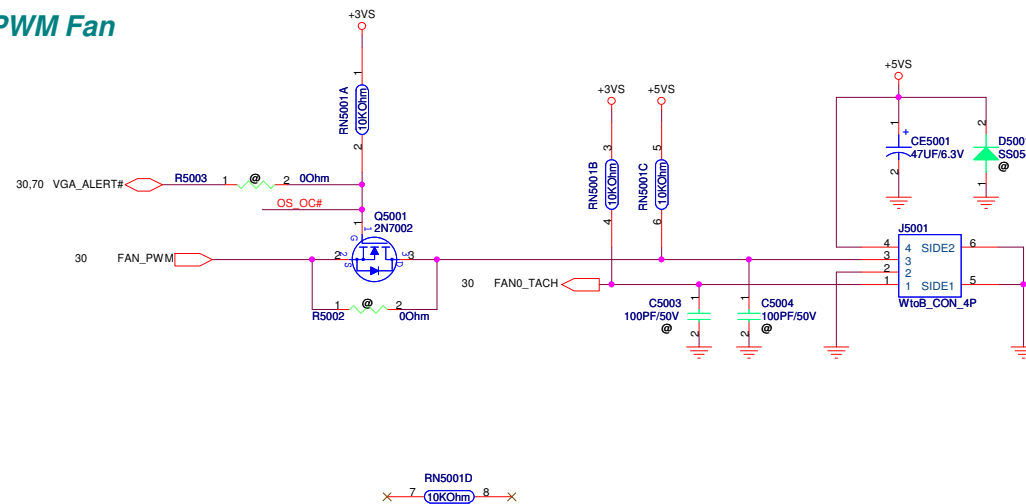
CPU Thermal Sensor

If support DC, Mount Block A and C, Unmount Block B;
If support QC, Mount Block B and C, Unmount Block A
200811121042



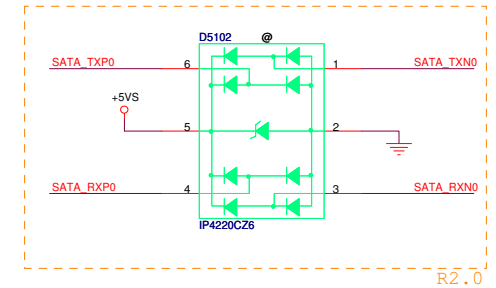
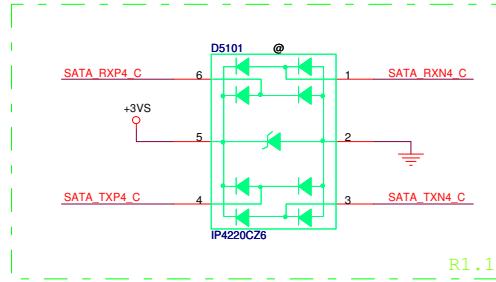
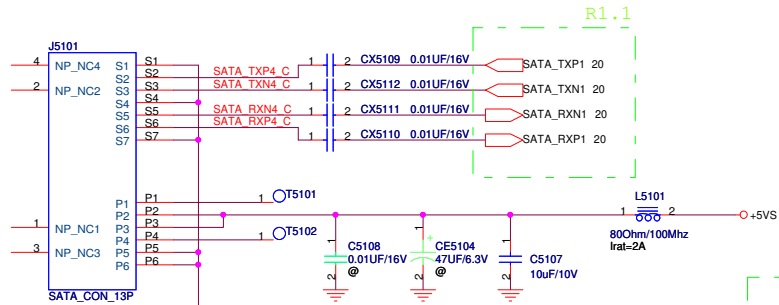
G50V and M52VF Mount R5004, R5005, R5006
C5005, C5006 although only support DC,
They can be cost down if only support DC

PWM Fan

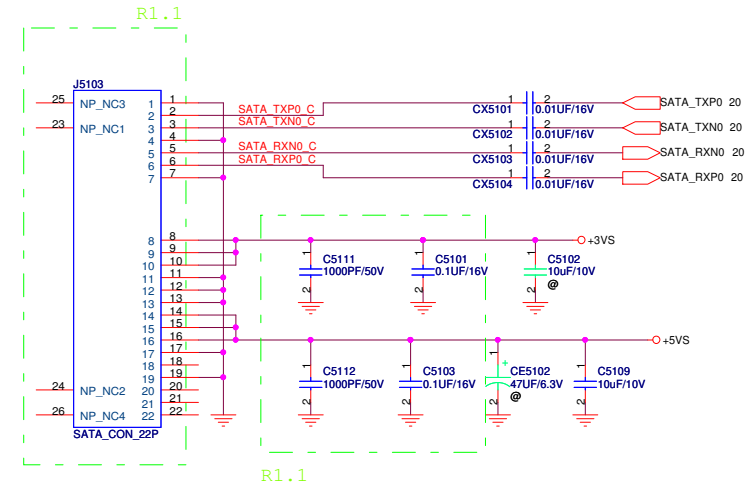


PEGATRON		Title : FAN_Fan & Sensor	
Pegatron BU2 HW Team 3		Engineer: Kevin1_Guo	
Size	Project Name	Rev	
Custom	G60VX	R 1.2	
Date: Wednesday, April 08, 2009		Sheet	50 of 100

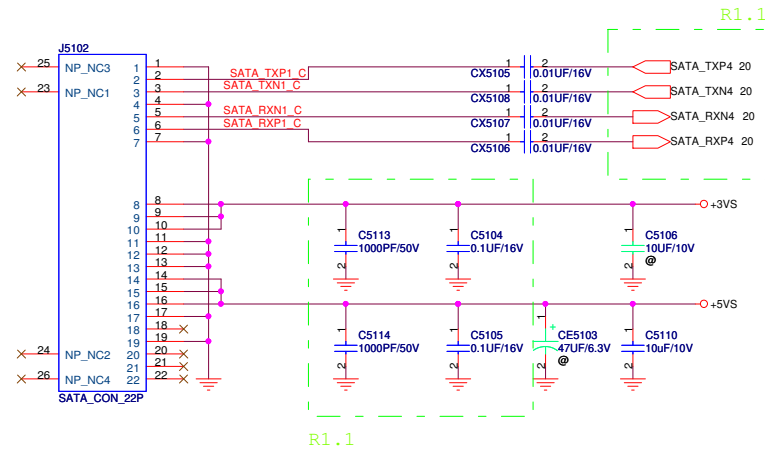
ODD



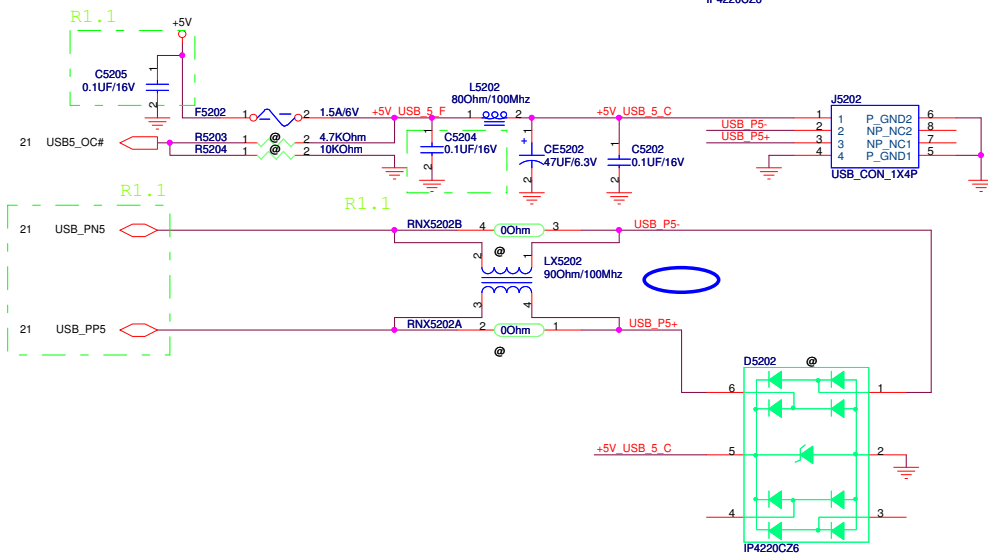
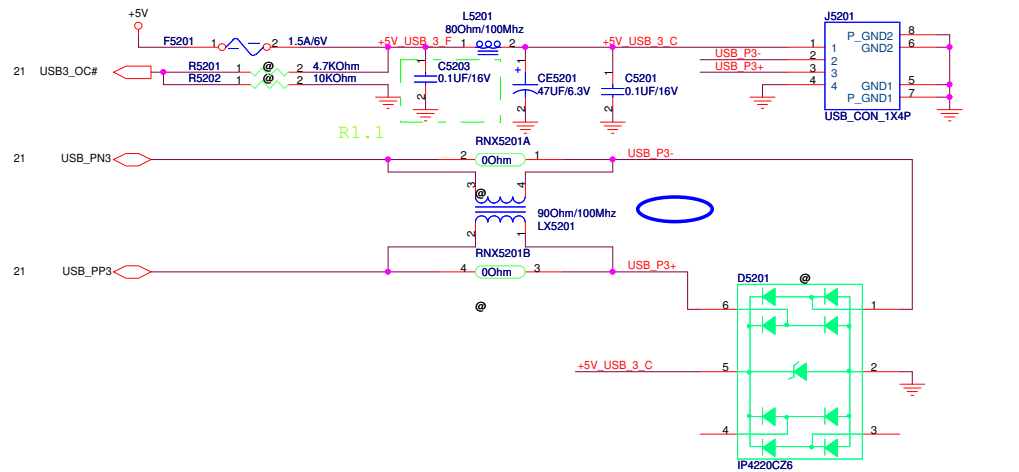
HDD



mount CE5102 C5103, unmount C5111
C5101 C5112 C5109
G60VX R2.0 costdown 20090402



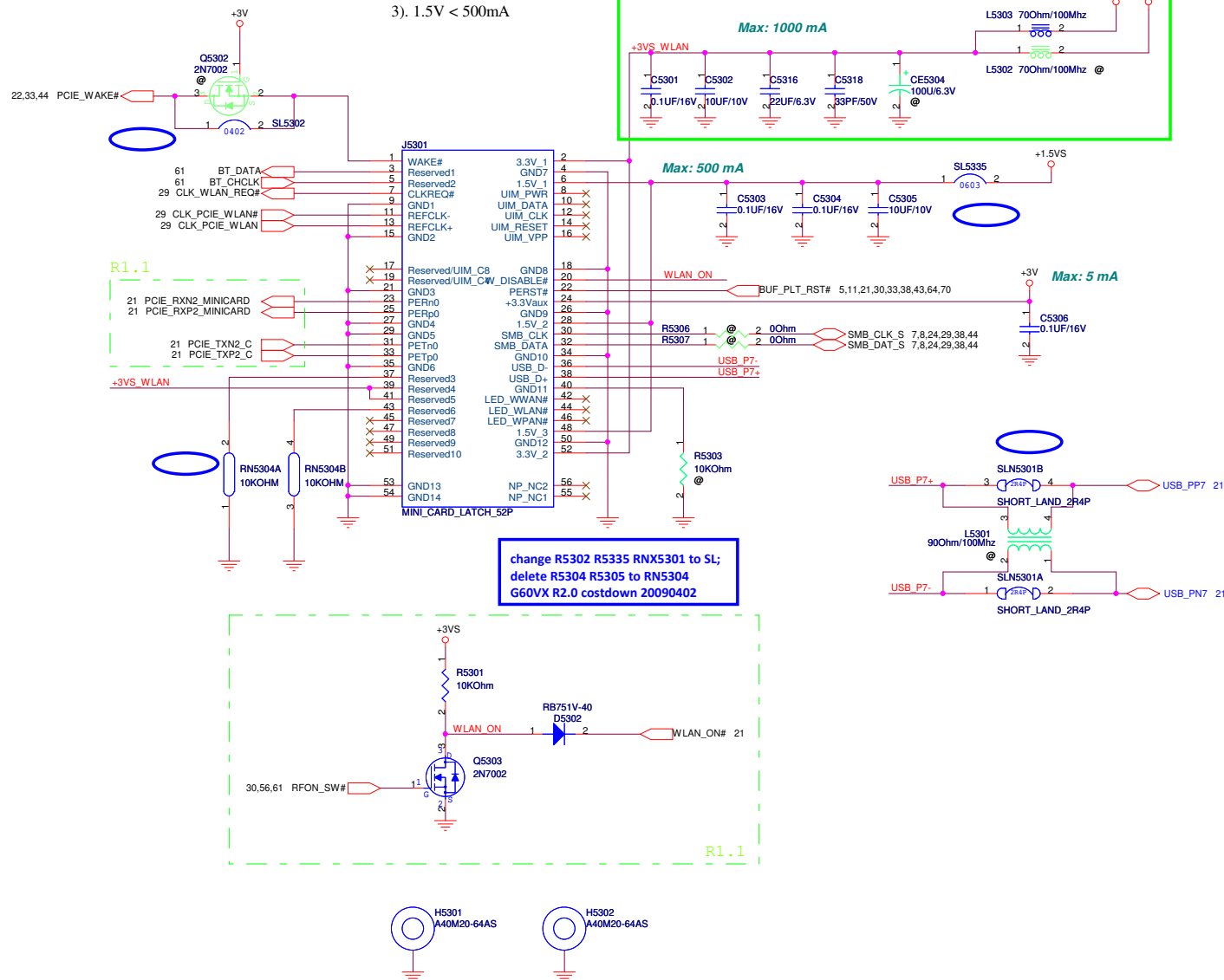
mount CE5103 C5105, unmount C5113
C5104 C5114 C5110
G60VX R2.0 costdown 20090402



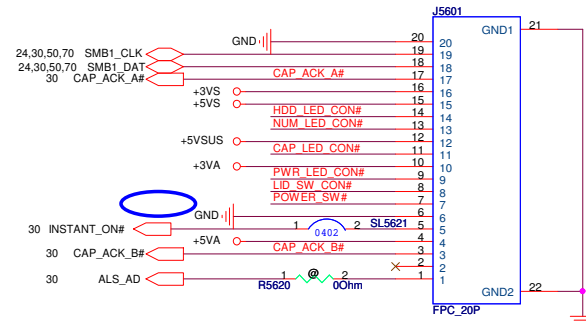
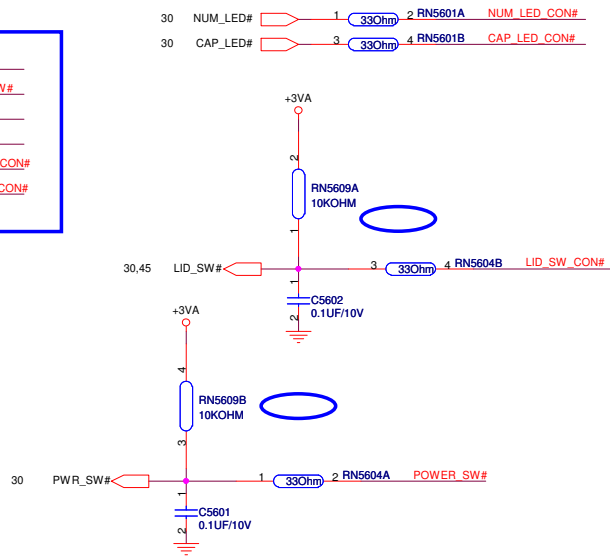
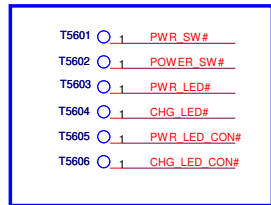
POWER CONSUMPTION:

- 1). 3V Main < 1000mA
- 2). 3V Aux < 250mA
- 3). 1.5V < 500mA

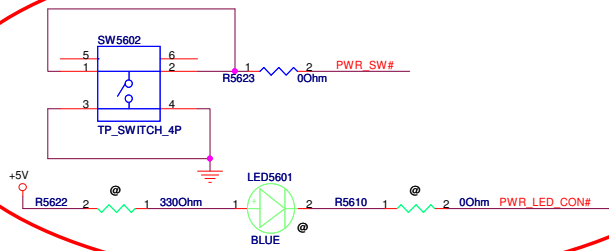
Follow H15HV R2.1 to accommodate large current
for Intel WiFi link 5300/5100 WLAN card
G60VX R1.2 20090305



PEGATRON		Title : BAR ****	
Pegatron BU2 HW Team 3		Engineer: Kevin1_Guo	
Size	Project Name		Rev
Custom	G60VX		R 1.2
Date: Thursday, March 05, 2009		Sheet	54 of 100

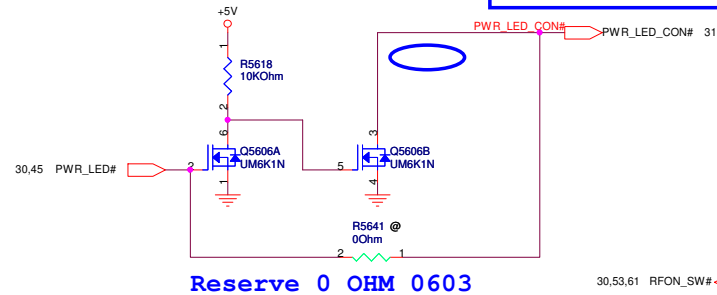


For Test

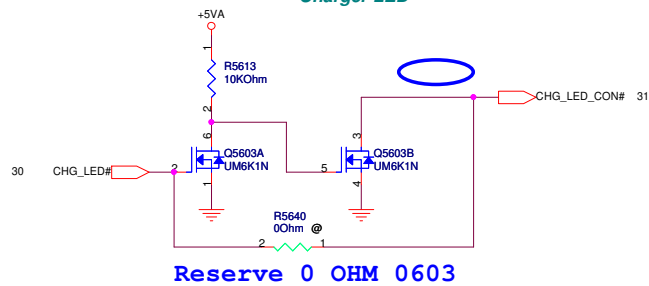


Power LED

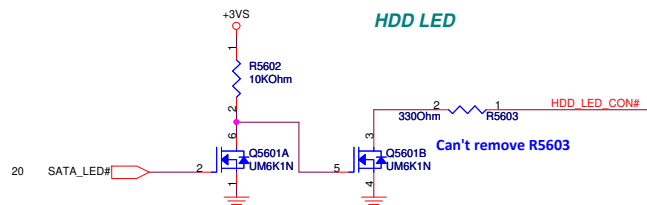
delete R5609 R5607, add RN5609
 delete R5621
 delete R5619
 delete R5614
 delete R5617 R5616
 G60VX R2.0 costdown 20090402



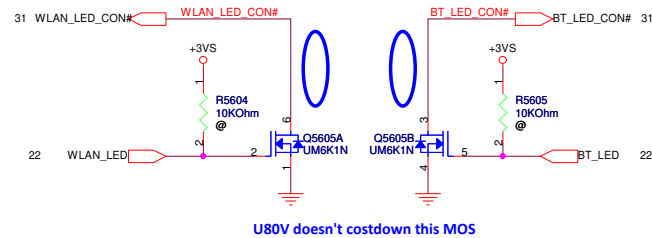
Charger LED



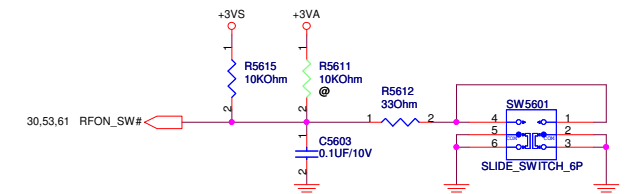
HDD LED



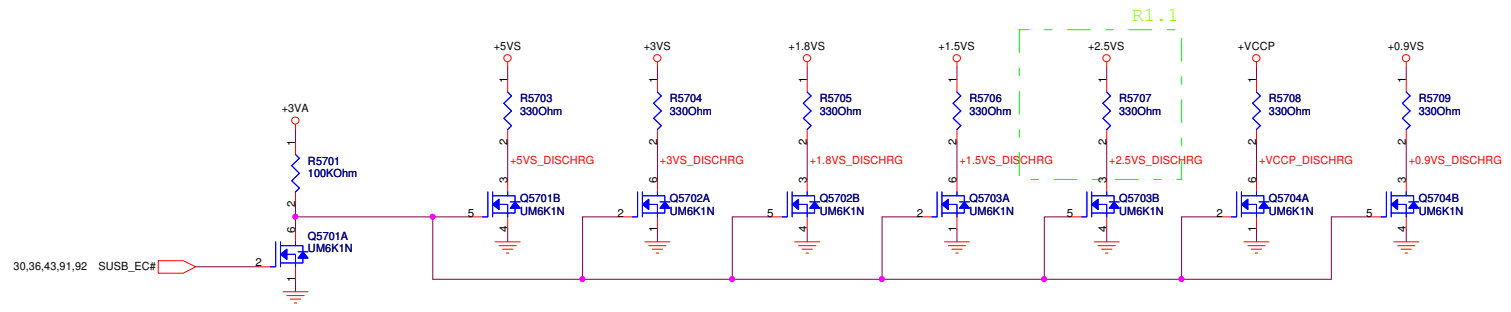
WLAN LED



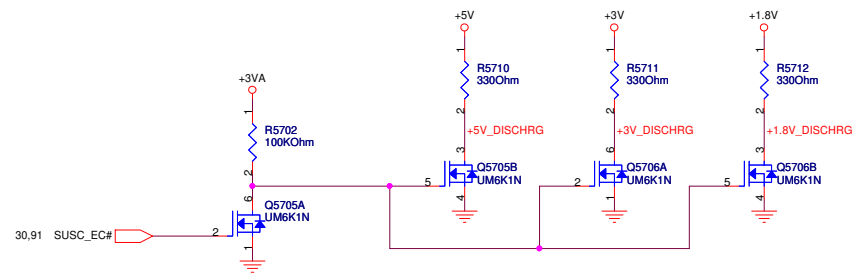
BT LED



PEGATRON		Title : <u>LED_Indicator</u>	
<u>Pegatron BU2 HW Team 3</u>		Engineer: <u>Kevin1_Guo</u>	
Size	Project Name	Rev	
Custom	G60VX	R 1.2	
Date:	Wednesday, April 08, 2009	Sheet	56 of 100

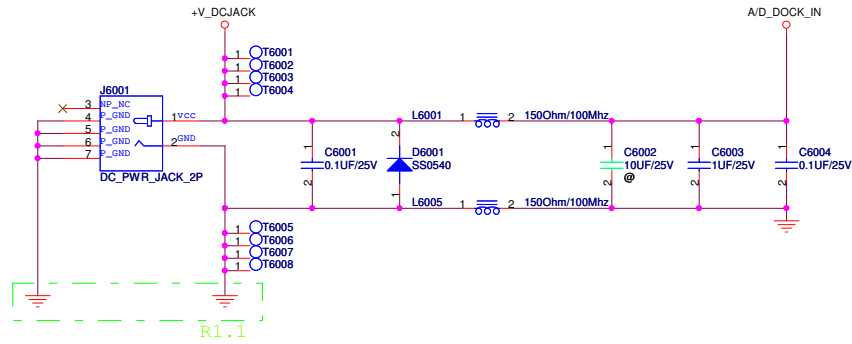


Need to verification!
G60VX R2.0 costdown 20090402

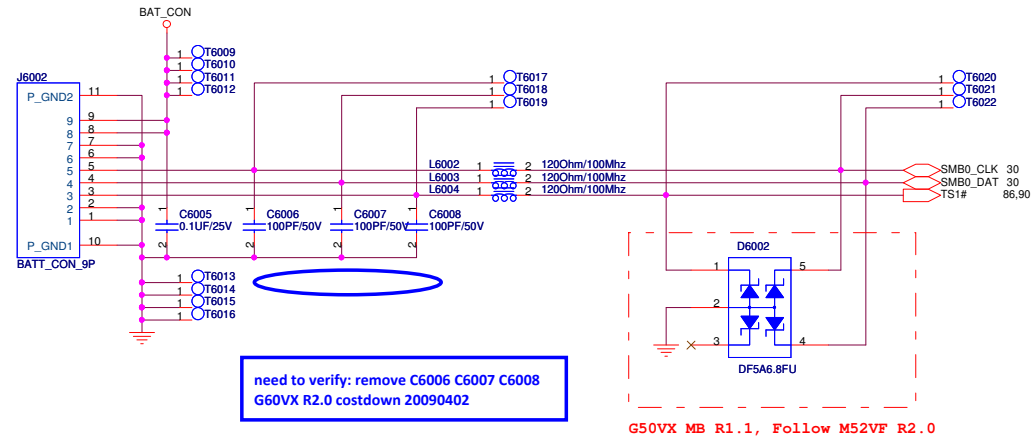


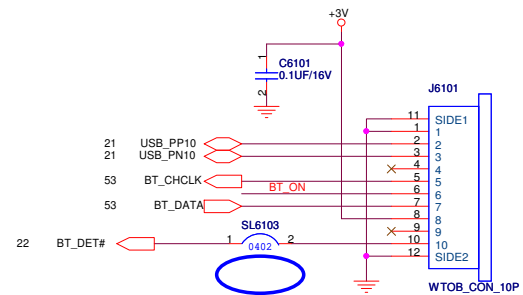
PEGATRON		Title : pci ****	
Pegatron BU2 HW Team 3		Engineer: Kevin1_Guo	
Size	Project Name		Rev
Custom	G60VX		R 1.2
Date: Thursday, March 05, 2009		Sheet	58 of 100

DC Jack

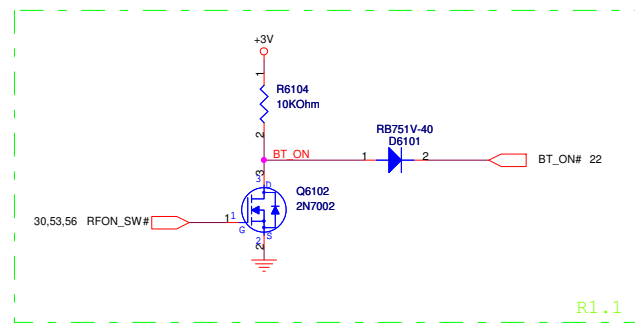


Battery Connector



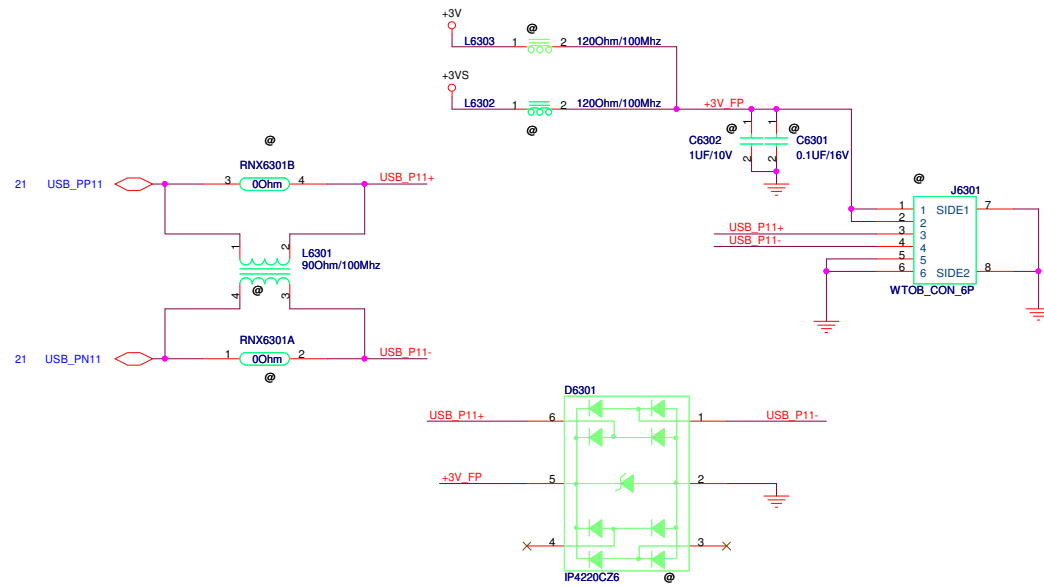


delete R6103
G60VX R2.0 costdown 20090402



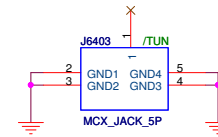
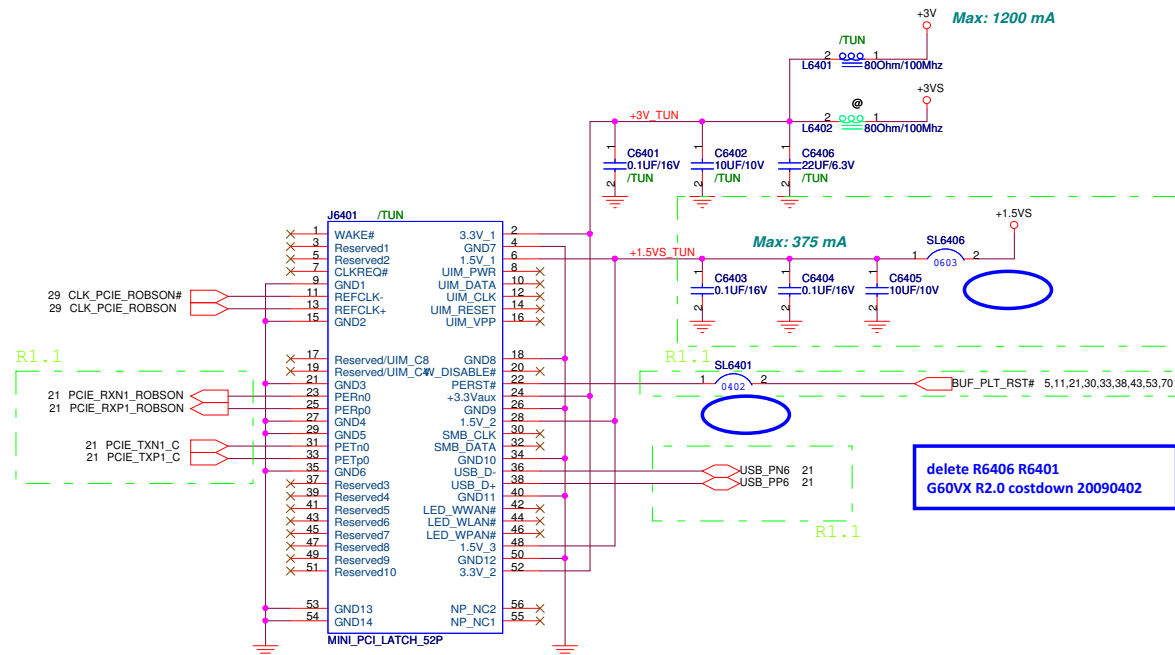
R1.1

PEGATRON		Title : TPM ****	
Pegatron BU2 HW Team 3		Engineer: Kevin1_Guo	
Size	Project Name		Rev
Custom	G60VX		R 1.2
Date: Thursday, March 05, 2009		Sheet	62 of 100

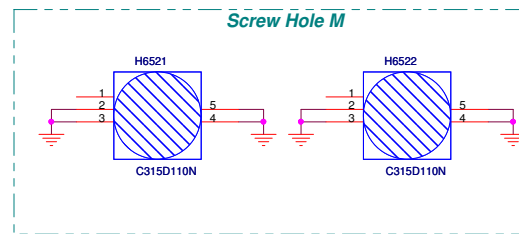
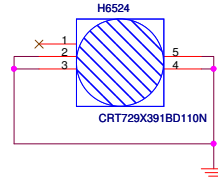
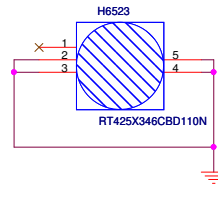
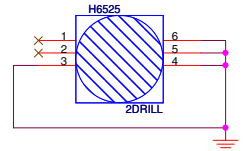
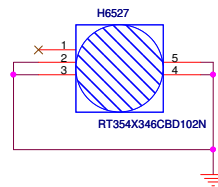
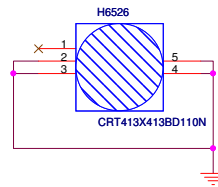
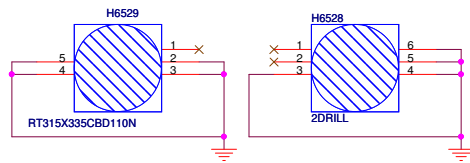
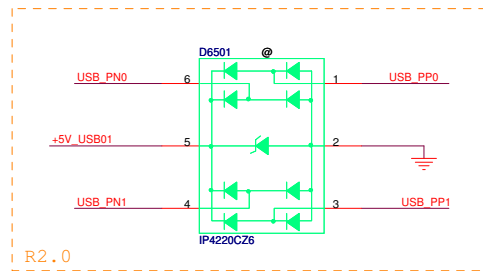
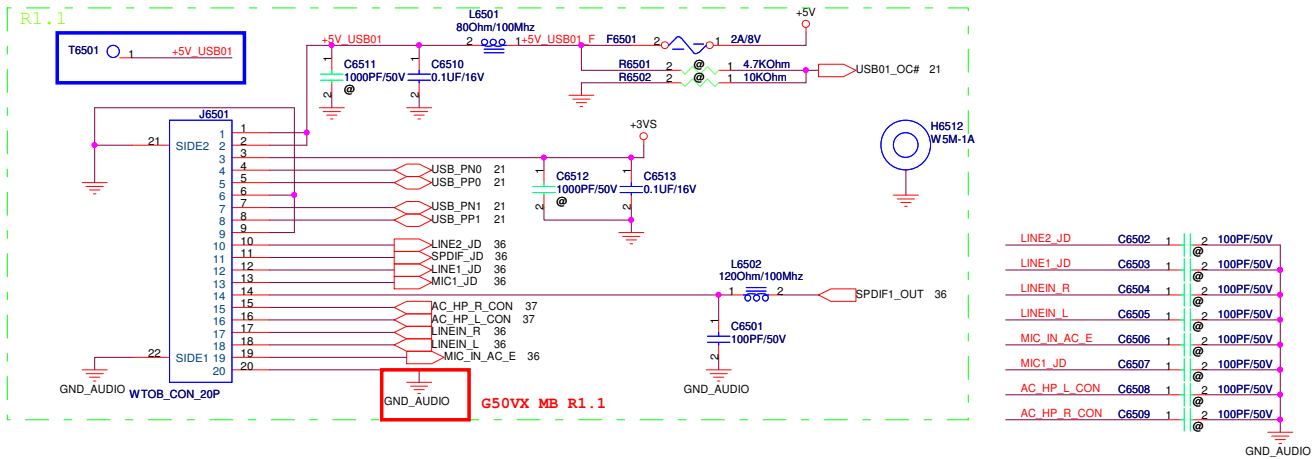


R2.0

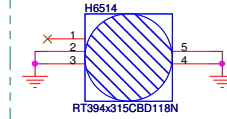
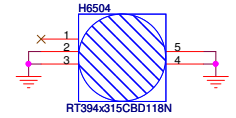
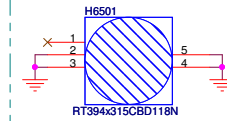
```
Unmount J6301, C6301, C6302, L6302
RXN6301 for delete FP connector
L6303, L6301, D6301 is reserved
200811102025
```



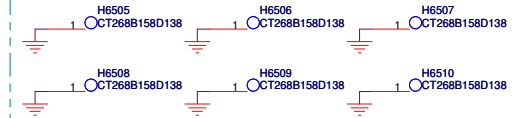
PEGATRON		Title : TUN_TV Tuner	
Pegatron BU2 HW Team 3		Engineer: Kevin1_Guo	
Size	Project Name	Rev	R 1.2
Custom	G60VX		
Date: Wednesday, April 08, 2009	Sheet 64 of 100		



Screw Hole A



Screw Hole B



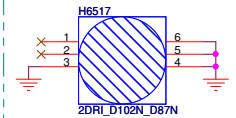
Screw Hole C

Screw Hole F

Screw Hole H

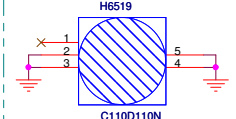
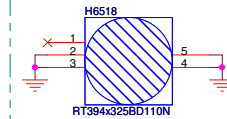
Screw Hole I

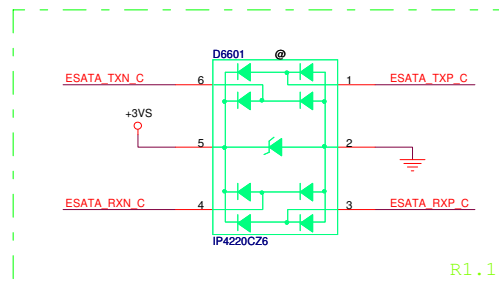
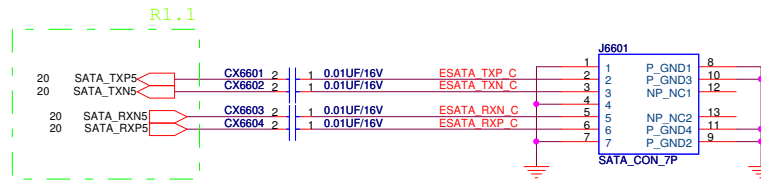
Screw Hole J

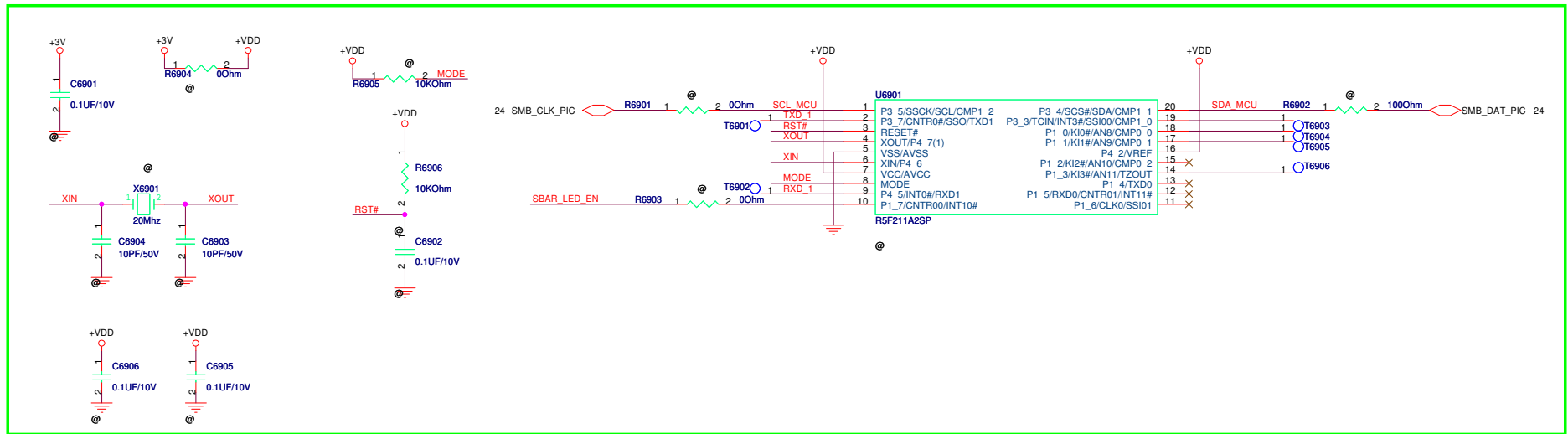


Screw Hole K

Screw Hole L

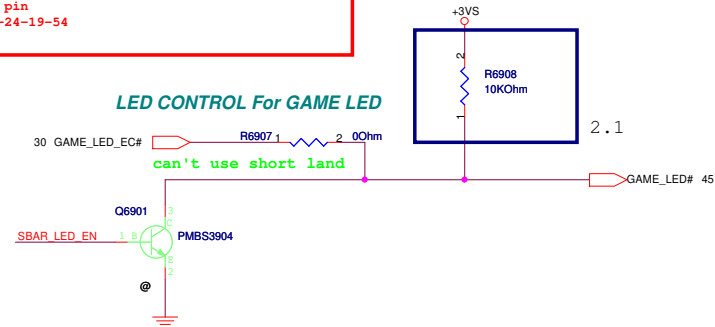






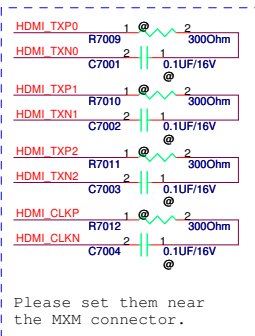
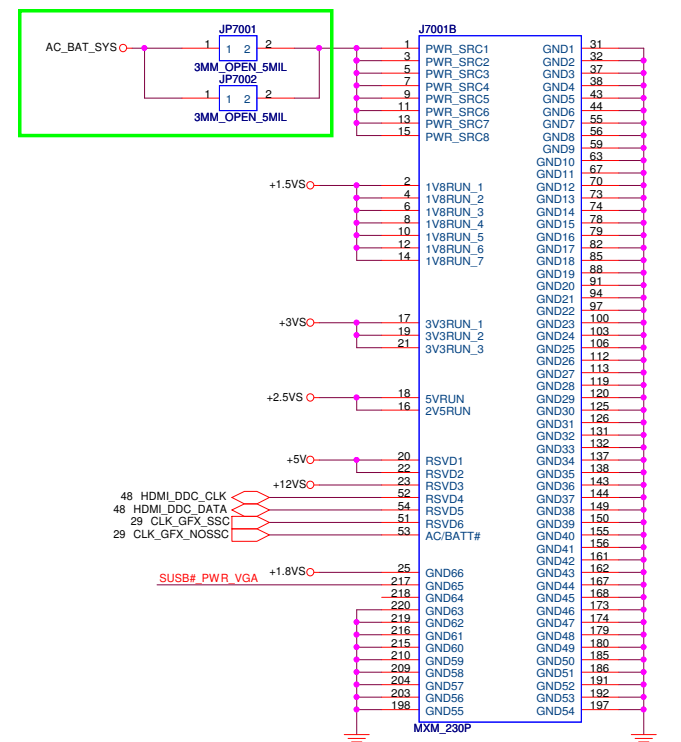
Cause EC will control GAME_LED#
Mount R6907 R6908, unmount
all others and Q2402 RN2402
G60VX R1.2 20090305

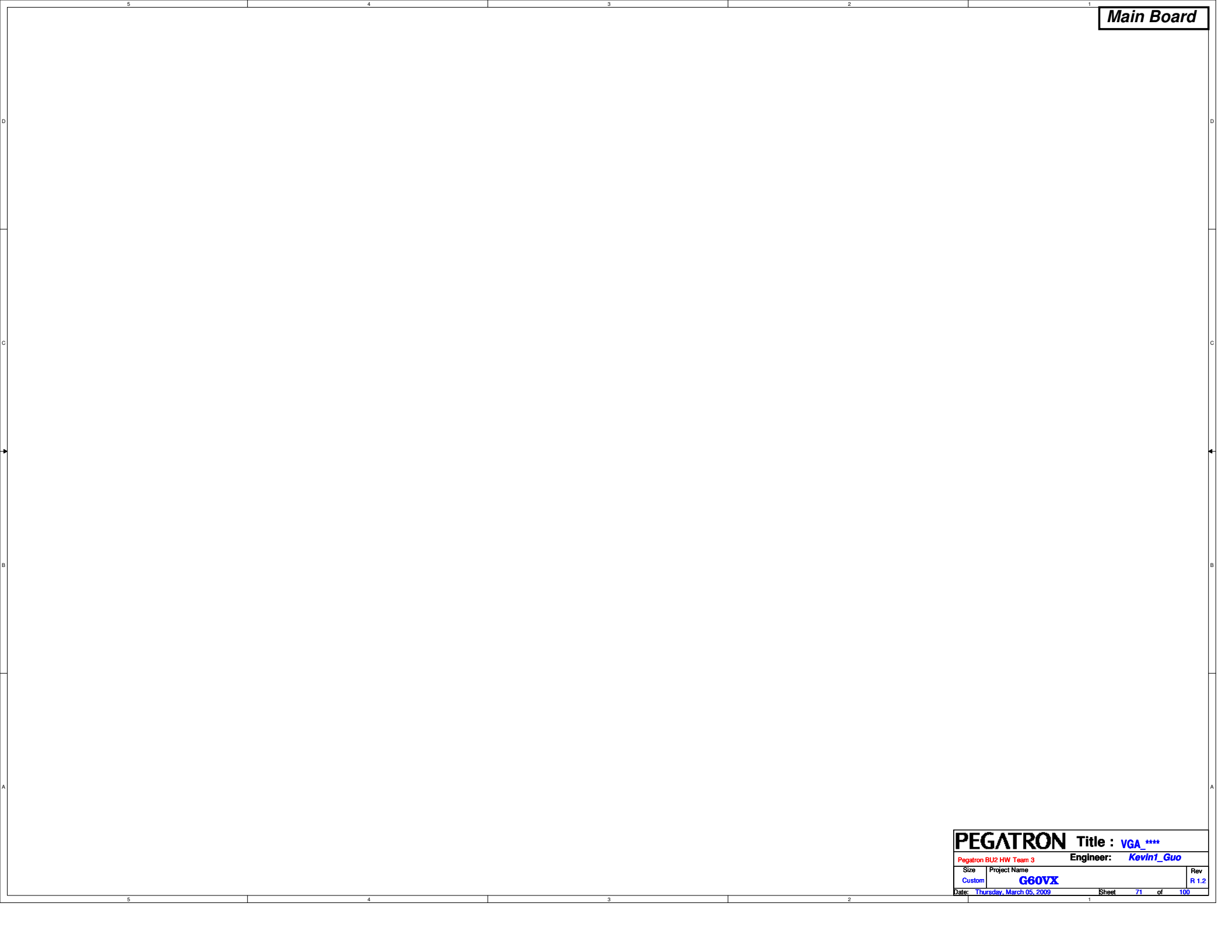
G50VX V1.0, Change net GAME_LED_EC# from
connecting with EC.GPA3 pin to connecting with
EC.GPA6 pin
2008-11-24-19-54



PCIEB_RXN[15:0] 11
PCIEB_RXP[15:0] 11
PCIEG_RXN[15:0] 11
PCIEG_RXP[15:0] 11

delete co-lay, reserved bead for EMI,
G60VX R2.0 20090408



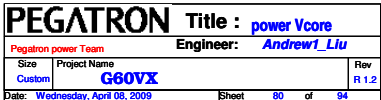


PEGATRON		Title : VGA ****	
Pegatron BU2 HW Team 3		Engineer: Kevin1_Guo	
Size	Project Name		Rev
Custom	G60VX		R 1.2
Date: Thursday, March 05, 2009		Sheet	72 of 100

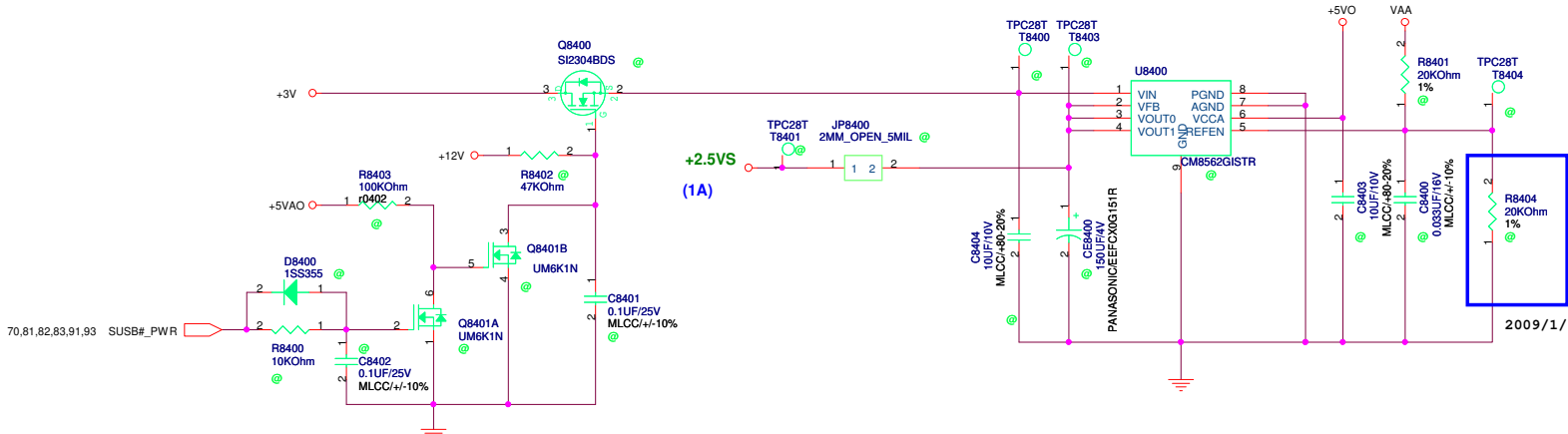
PEGATRON		Title : VGA ****	
Pegatron BU2 HW Team 3		Engineer: Kevin1_Guo	
Size	Project Name		Rev
Custom	G60VX		R 1.2
Date: Thursday, March 05, 2009		Sheet	74 of 100

PEGATRON		Title : VGA ****	
Pegatron BU2 HW Team 3		Engineer: Kevin1_Guo	
Size	Project Name		Rev
Custom	G60VX		R 1.2
Date: Thursday, March 05, 2009		Sheet	76 of 100

PEGATRON		Title : VGA ****	
Pegatron BU2 HW Team 3		Engineer: Kevin1_Guo	
Size	Project Name		Rev
Custom	G60VX		R 1.2
Date: Thursday, March 05, 2009		Sheet	78 of 100



+2.5VS



2009/1/13

+1.5VO: ROCSET = R8213 ; R8215 = R8213=10KOhm
+1.05VO: ROCSET = R8212 ; R8212=R8211=10KOhm

$$\begin{aligned} +1.5\text{VO} &= \text{VREF} * (\text{R8206} + \text{R8214}) / \text{R8214} = 1.52\text{V} \pm 2.26\% \\ +1.05\text{VO} &= \text{VREF} * (\text{R8207} + \text{R8210}) / \text{R8207} = 1.052\text{V} \pm 1.9\% \end{aligned}$$

```
+1.5VO: Rfset =R8204; Fsw=360KHz
+1.05VO: Rfset =R8202; Fsw=300KHz
```

The diagram illustrates a complex PCB layout for a power supply system, featuring a multi-output design. The layout is organized into several functional blocks:

- Input Section:** Includes a USB power input (SUSB#_PWR) and a main power input (AC_BAT_SYS). The USB input is connected to a USB connector (U8200B) and a USB power switch (D8201, T8201). The main power input is connected to a power switch (D8201, T8201) and a power filter (R8201, C8201).
- Regulation Section:** Features a voltage regulator (U8200A) and a feedback network (R8202, C8202). The regulator is connected to a feedback network (R8202, C8202) and a feedback network (R8202, C8202).
- Output Section:** Includes a multi-output distribution section with multiple outputs (e.g., +1.05V, +1.5V, +VCCP). The outputs are connected to a multi-output distribution section (U8200B) and a multi-output distribution section (U8200B).
- Passive Components:** The layout includes numerous capacitors (C8201-C8229) and resistors (R8201-R8229) for filtering, decoupling, and signal conditioning.
- Connectors:** The layout includes a USB connector (U8200B) and a multi-pin connector (U8200A).

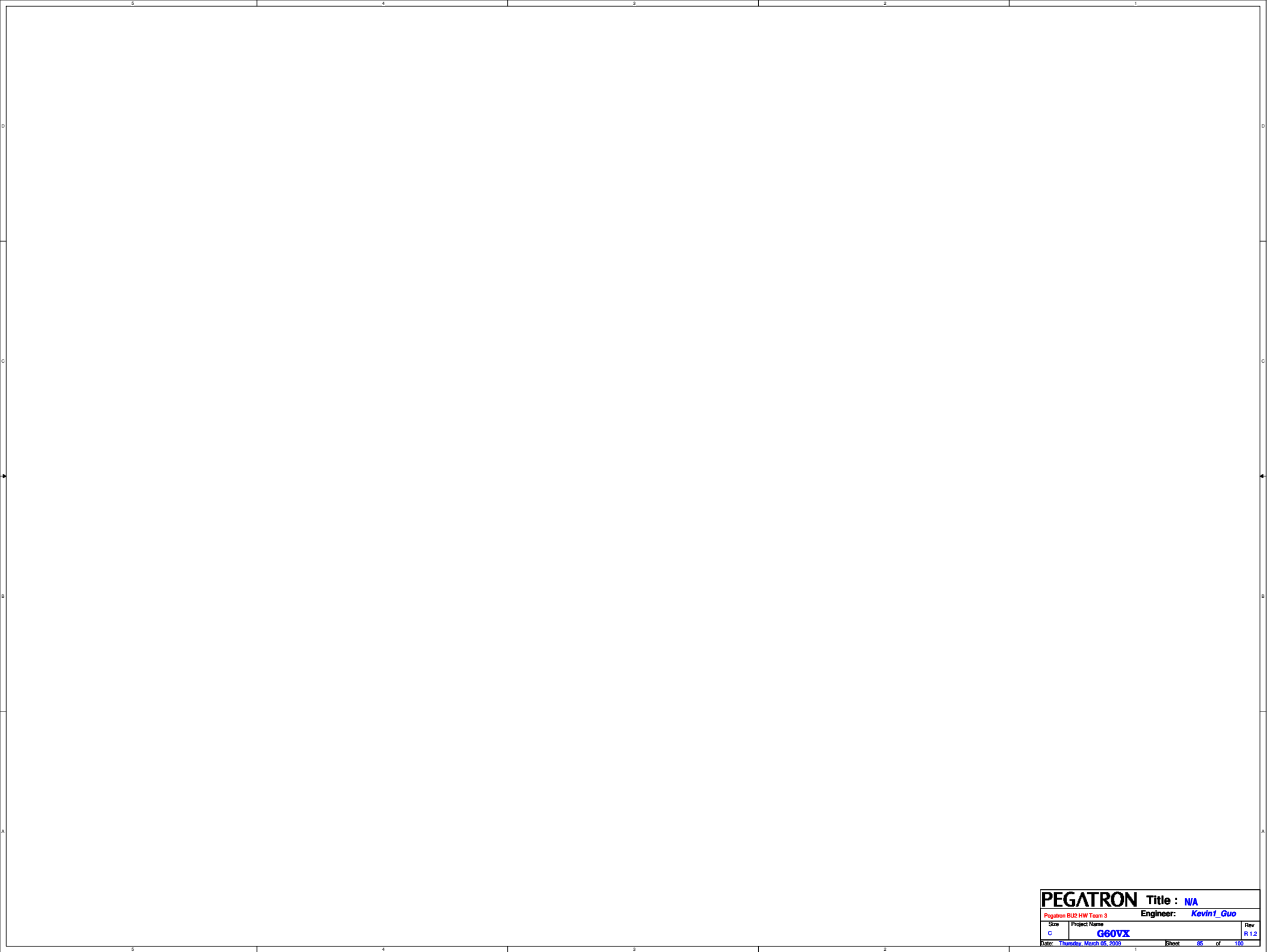
The layout is color-coded with red for power planes and green for signal planes. A legend at the bottom right identifies the components and their values:

Size	Project Name	Rev
Custom	G60Vx	1.2

Date: Wednesday, April 08, 2009 Sheet 62 of 94

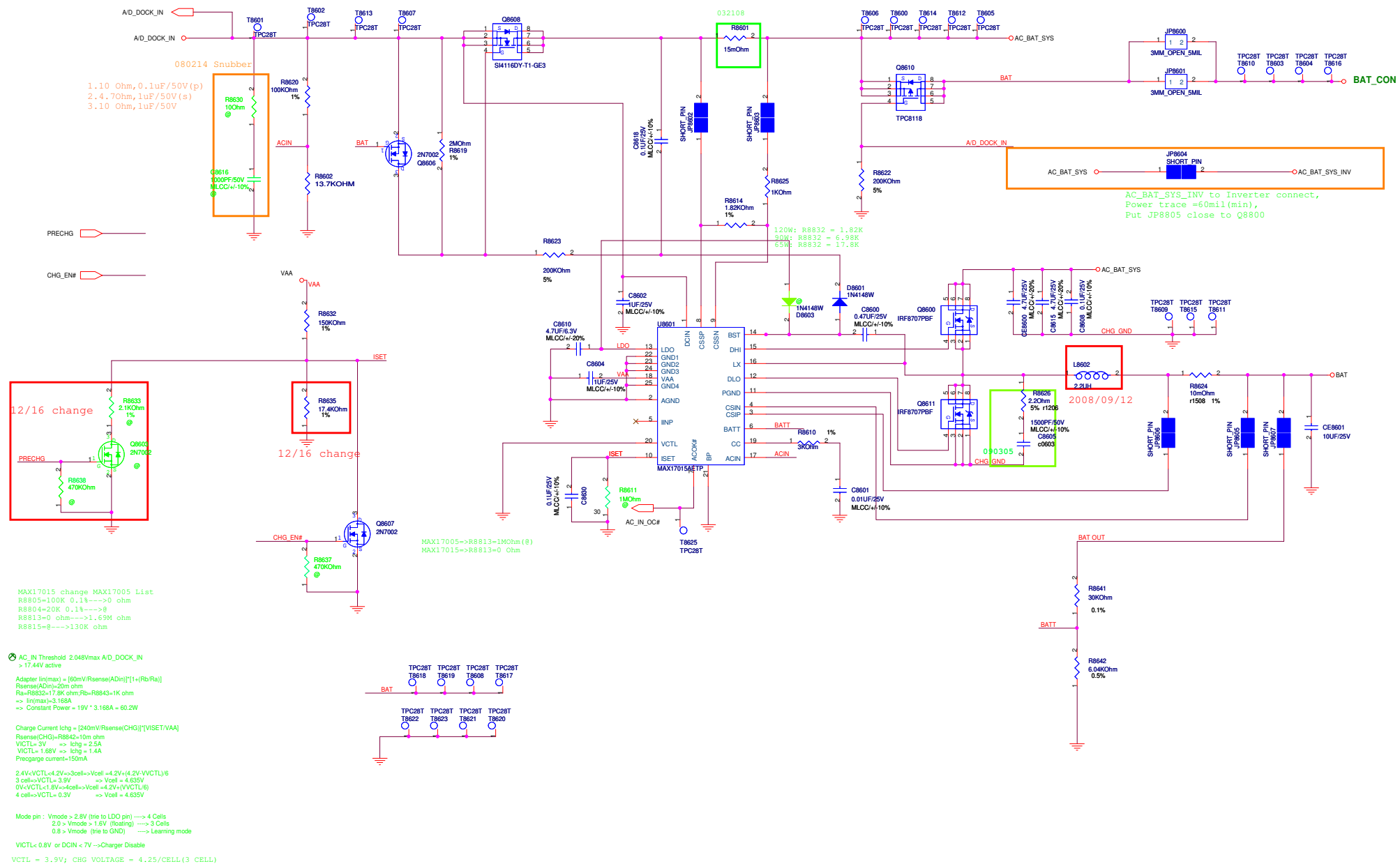
PEGATRON		Title : <i>POWER_I/O_1.5VS & 1.0VS</i>	
		Engineer: <i>Andrew T. Liu</i>	
Size <i>Custom</i>	Project Name G60Vx		Rev 1.2
Date: <i>Wednesday, April 08, 2009</i>	Sheet	82	of 94

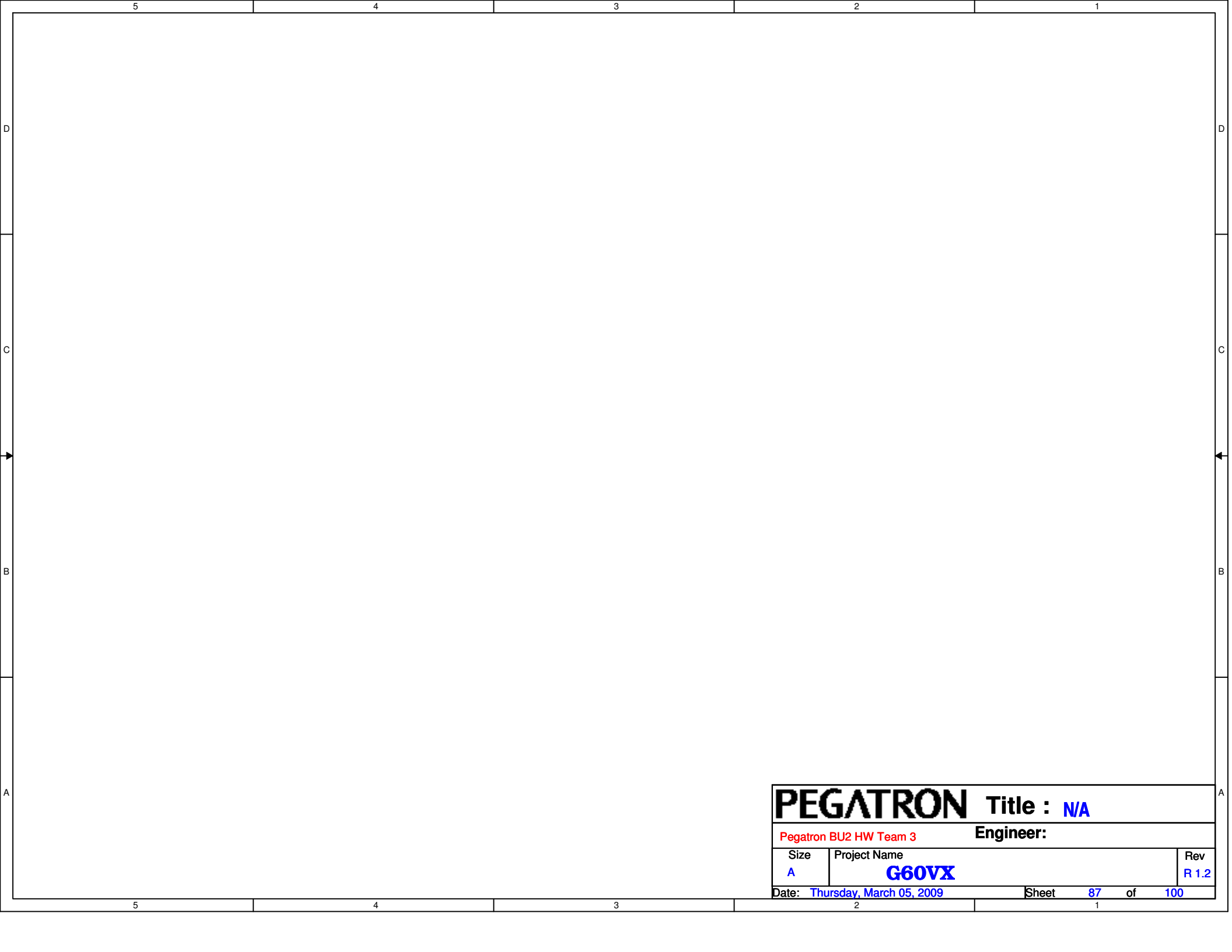




PEGATRON		Title : N/A	
Pegatron BU2 HW Team 3		Engineer: Kevin1_Guo	
Size	Project Name		Rev
C	G60VX		R 1.2
Date: Thursday, March 05, 2009		Sheet	65 of 100

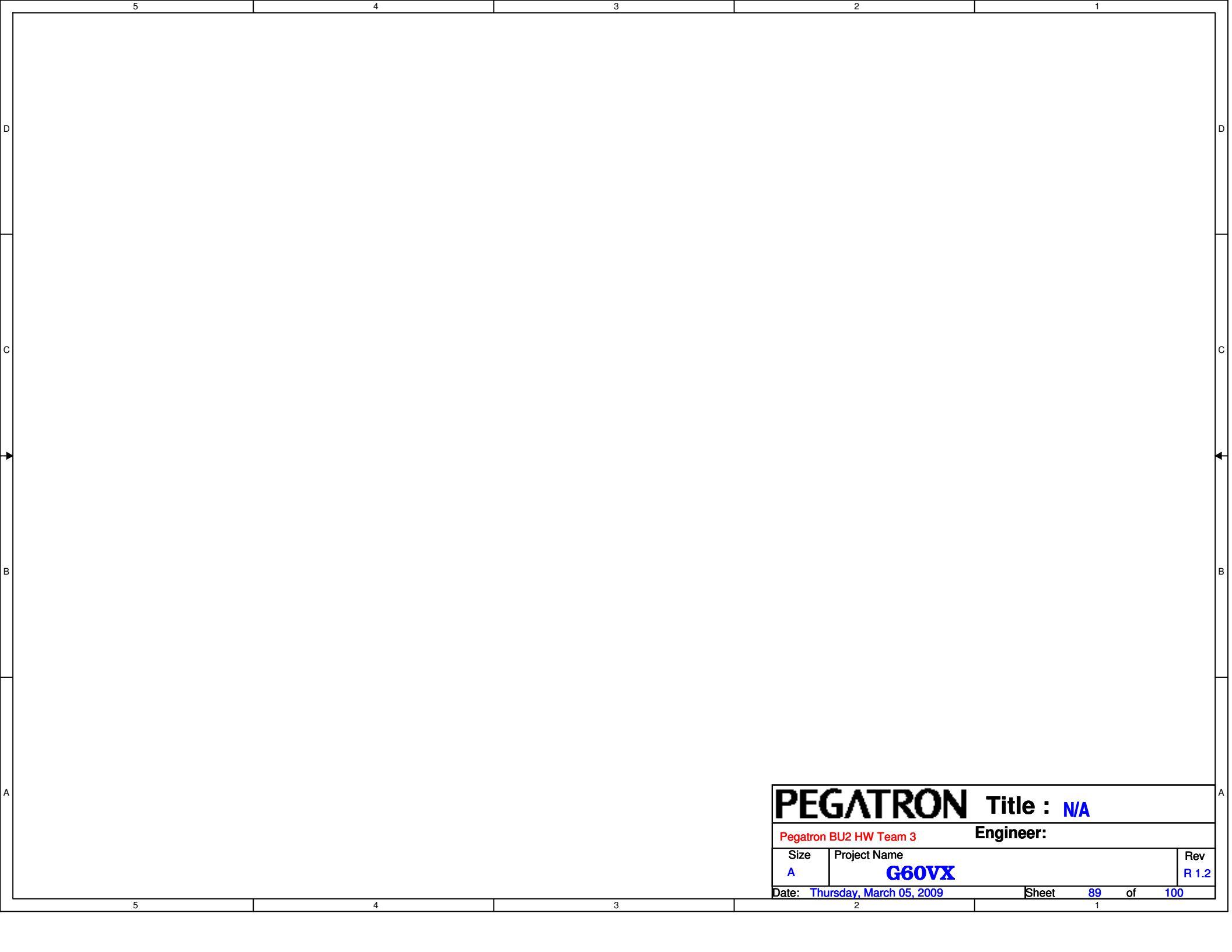
POWER PATH & BAT_LEARN





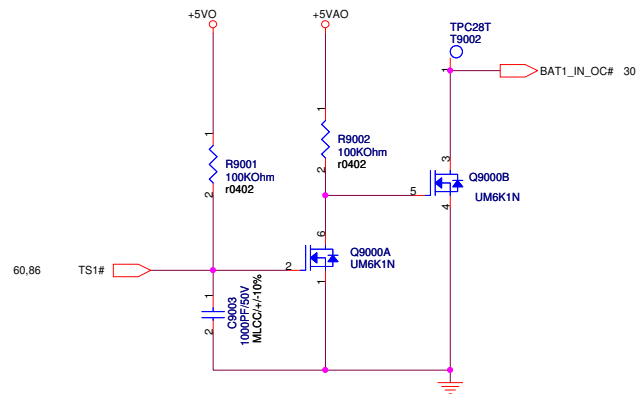
PEGATRON			Title : N/A		
Pegatron BU2 HW Team 3			Engineer:		
Size	Project Name				Rev
A	G60VX				R 1.2
Date: Thursday, March 05, 2009			Sheet	87	of 100

5	4	3	2	1
D				D
C				C
B				B
A				A
<div> <div> <div>PEGATRON</div> <div> <div>Pegatron BU2 HW Team 3</div> <div> <div>Size</div> <div>A</div> </div> </div> <div> <div>Project Name</div> <div>G60VX</div> </div> <div> <div>Date: Thursday, March 05, 2009</div> <div> <div>Sheet</div> <div>88</div> <div>of</div> <div>100</div> </div> </div> </div> </div>				<div> <div>Title : N/A</div> <div>Engineer:</div> </div>



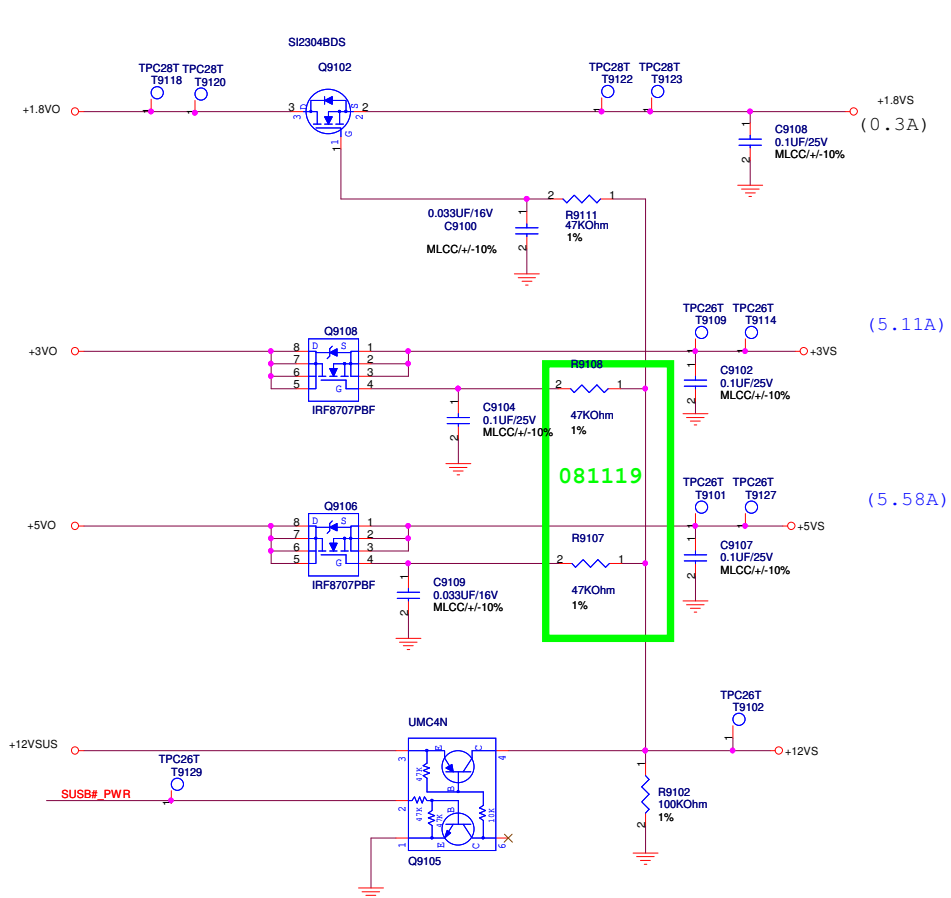
PEGATRON			Title : N/A		
Pegatron BU2 HW Team 3			Engineer:		
Size	Project Name				Rev
A	G60VX				R 1.2
Date: Thursday, March 05, 2009			Sheet	89	of 100

BATTERY IN DETECT

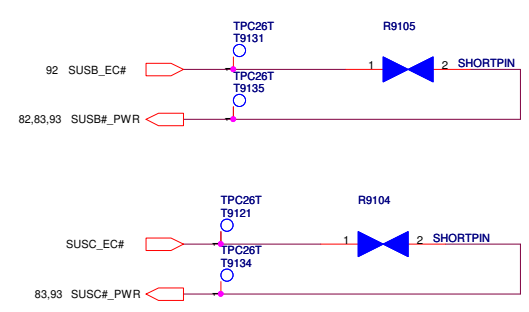
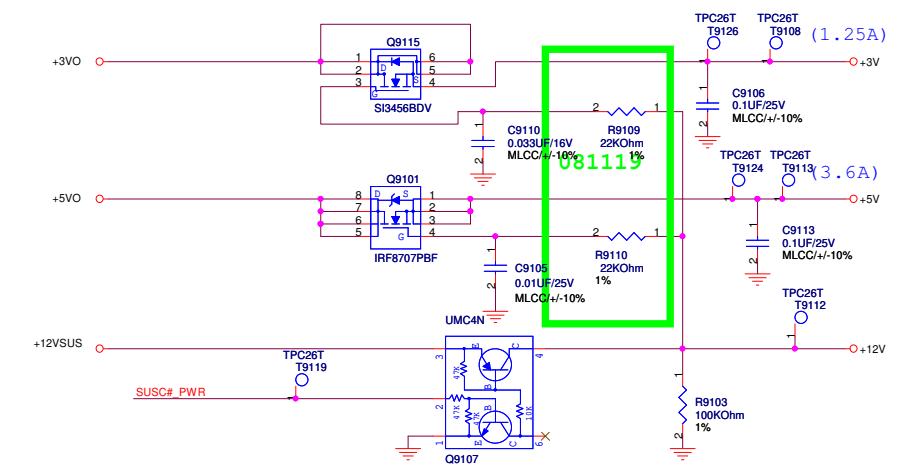


PEGATRON		Title : POWER_DETECT	
Pegatron power Team		Engineer: Andrew1_Liu	
Size Custom	Project Name G60VX		Rev R 1.2
Date: Wednesday, April 08, 2009		Sheet	90 of 94

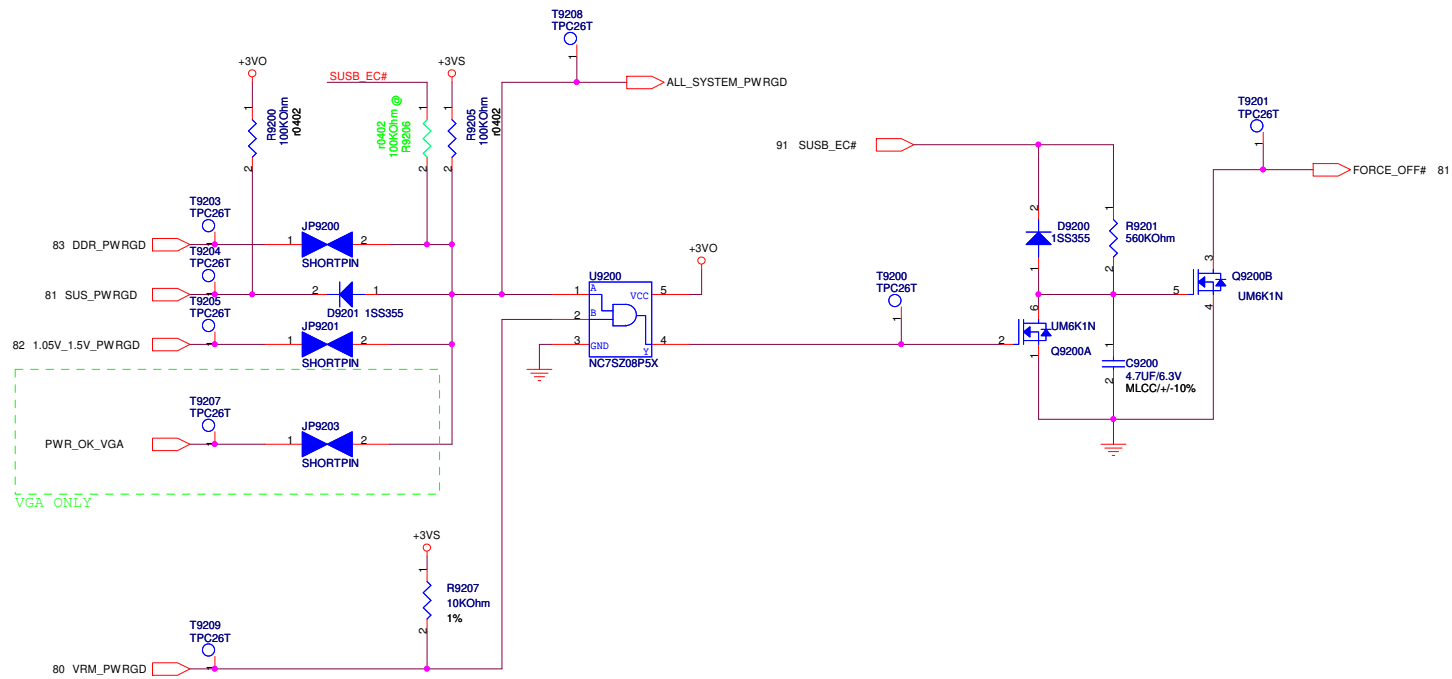
SUSB#_PWR POWER



SUSC#_PWR POWER



POWER GOOD DETECTOR



<Variant Name>

PEGATRON		Title :POWER_PROTECT	
Size		Engineer: Andrew1_Liu	
Custom	Project Name	G60Vx	
Date: Wednesday, April 08, 2009	Sheet	92	of 94
Rev		1.2	

AC_BAT_SYS ○ → AC_BAT_SYS 80,81,82,83,88
BAT ○ → BAT 88
BAT_CON ○ → BAT_CON 88

+3VA ○ → +3VA 81
+5VAO ○ → +5VAO 81,90
+5VA ○ → +5VA 81

+5VO ○ → +5VO 81,82,83,90,91
+3VO ○ → +3VO 81,91
+1.8VO ○ → +1.8VO 83
+0.9VO ○ → +0.9VO 83
+1.05VO ○ → +1.05VO 80,82
+1.5VO ○ → +1.5VO 82

+5VSUS ○ → +5VSUS 81
+3VSUS ○ → +3VSUS 81,92
+12VSUS ○ → +12VSUS 81,91

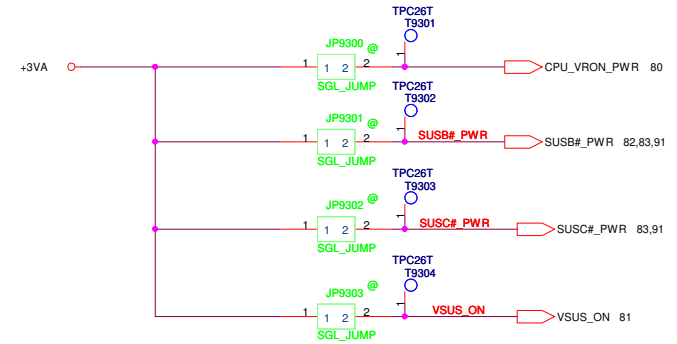
+5V ○ → +5V 91
+3V ○ → +3V 91
+12V ○ → +12V 91
+1.8V ○ → +1.8V 83

+3VS ○ → +3VS 80,91,92
+5VS ○ → +5VS 80,91
+12VS ○ → +12VS 91

+1.5VS ○ → +1.5VS 82
+0.9VS ○ → +0.9VS 82
+1.8VS ○ → +1.8VS 82

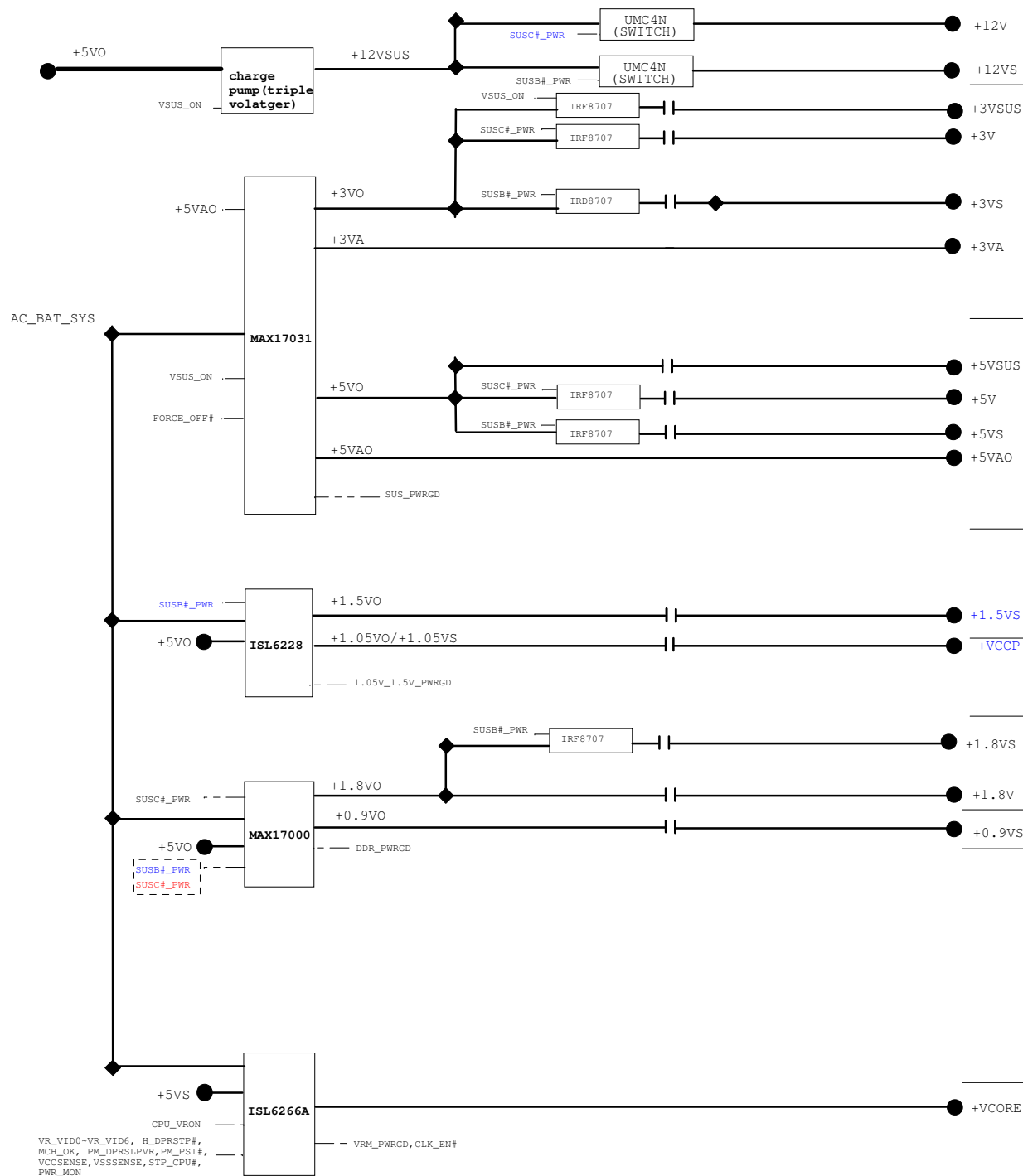
+VCCP ○ → +VCCP 82
+VCORE ○ → +VCORE 80

FOR POWER TEST

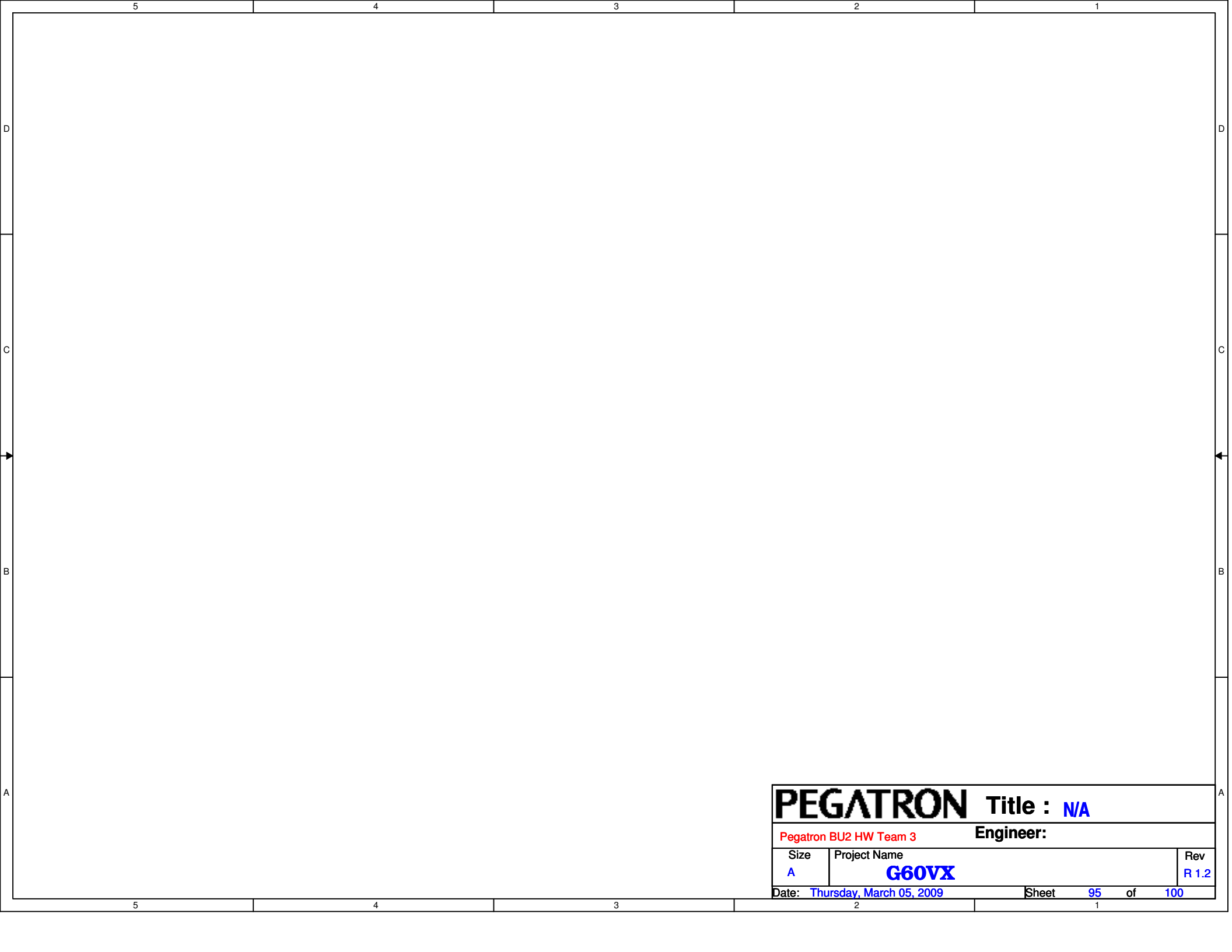


<Variant Name>

PEGATRON		Title :POWER SIGNAL	
		Engineer: Andrew1_Liu	
Size	Project Name	Rev	
Custom	G60Vx	1.2	
Date: Wednesday, April 08, 2009	Sheet	93	of 94



		Design rating
(10mA)	(20mA)	
(10mA)		
(0.74A)		
(1.29A)		
(8.62A)	(10.783A)	
(0.133A)		
(0.01A)		
(3.61A)		
(3.875A)	(7.495A)	
(0.01A)		
(3.77A)	(3.77A)	
(12.816A)	(12.816A)	
(11.96A)	(11.96A)	
(2A)	(2A)	
(47A)	(47A)	



PEGATRON			Title : N/A		
Pegatron BU2 HW Team 3			Engineer:		
Size	Project Name				Rev
A	G60VX				R 1.2
Date: Thursday, March 05, 2009			Sheet 95 of 100		

Rev	Date	Description
R1.0		First Release!
R1.1		

Rev	Date	Description

PEGATRON

Pegatron BU2 HW Team 3

Title : Revision History

Engineer:

Size

Custom

Project Name

G60VX

Date: Thursday, March 05, 2009

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Rev

R 1.2

R1.0

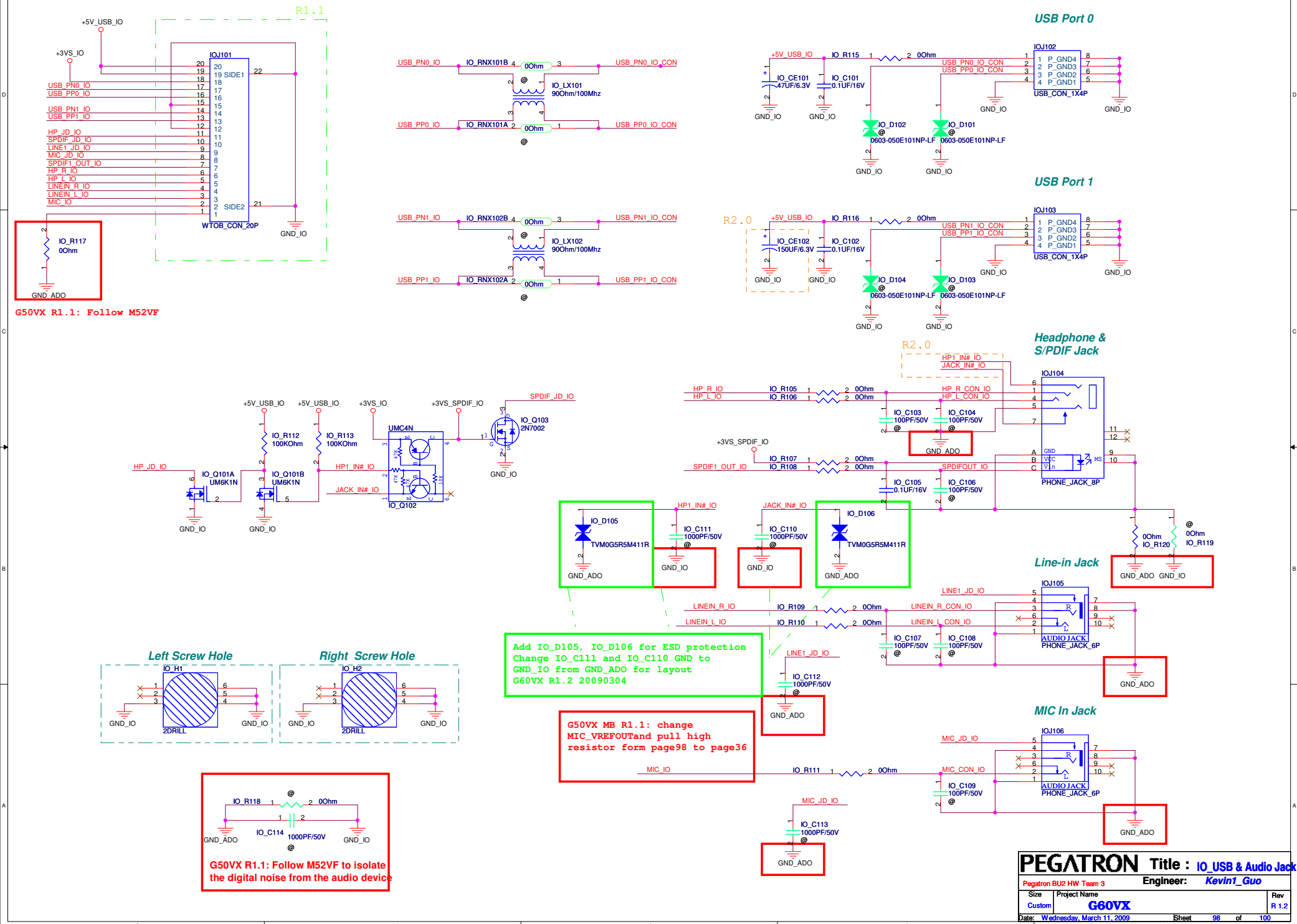
Item	Before	After	Reason	Owner	Date
	R8036:10.5k	R8036 change to 8.87k	To change VCORE load line to meet Intel spec.	Eve Kuo	2008/02/25
	R8015:0805	R8015 from 0805 --> 0603	0805 is common component to use.	Eve Kuo	2008/02/25
	Q8612, R8628, R8629	De-pop Q8612, R8628, R8629	G50V support 3S battery	Eve Kuo	2008/02/25

R1.1

Item	Before	After	Reason	Owner	Date
	JP8601,JP8606	Delete JP8601,JP8606	Due to the factory's requirement, the bead and jump won't be co-lay.		

R2.0

Item	Before	After	Reason	Owner	Date



R1.0
R1.1

G50VX

2008/02/18	1. Change the port of SATA ODD and SATA HDD to meet design IP. (Page 51) 2. Change SMBus of the Cap-sense Touch key from SMB0 to SMB1. (Page 56) 3. Correct the signals of ESATA. (Page 66) 4. Set R3318 as mount. (Page 33) 5. Correct the signals of PCIE of WLAN. (Page 53) 6. Correct the signals of PCIE of TV Tuner and add the reset signal for PCIE TV Tuner. Set the 1.5V power rail as mount. (Page 64) 7. Unmount pull up resistors of 1394_SCL and 1394_SDA. (Page 40) 8. Add common choke on CMOS for EMI requirement. (Page 45) 9. Correct the signals of Newcard Debug Card. (Page 44) 10. Change the R1407 to 1206 size. (Page 14)
2008/02/20	11. Change EC to 8512. (Page 30) 12. Pull BAT2_IN_OC# up to fix CHARGER_LED bug. (Page 30)
2008/02/21	13. Delete the LCD_BL_DA signal which is designed for Light Sensor. (Page 45) 14. Change the R4504 to 100K to fix LCD will display white screen when system boots. (Page 45) 15. Add uP schematic to control the Game LED for FM request. (Page 69 & 24)
2008/03/05	16. Add discharge circuit for 2.5VS (Page 57) 17. Change BT and WLAN ON/OFF control method (Page 53 and 61) 18. Add ESD Protected Diode on SATA ODD and E-SATA(Page 51 and 66)
2008/03/11	19. Change PEG CLK Source on Clock Gen(Page 29)
2008/03/14	20. Change TouchPad Connector. (Page 31)
2008/03/18	21. Add 2 diodes to follow EC suggestion. (Page 22) 22. Change the IO Connector. (Page 65, 98) 23. Change Power Circuit. (Page 80-94) 24. Exchange CLK_ICHPCI and CLK_KBCPCI to follow Design IP setting. (Page 30) 25. Swap USB Ports to follow Design IP. (Page 45, 52, 64, 68,)
2008/03/19	26. Add 0OHM resistor between thermal sensor and CPU to follow Intel Design Guide. (Page 50) 27. Add a N-MOS between U4401 and PCI_WAKE# to prevent system can't enter S4 which is waked by U4401. (Page 44)
2008/03/24	28. Add +3VSUS to NewCard Power Switch. (Page 43) 29. Change the pull-up power source of SMB1 to +3VS. (Page 30)
2008/03/26	30. Change HDD Connector. (Page 51) 31. Add EMI Solution on LVDS connector. (Page 45) 32. Change the Ground of DC Jack for EMI. (Page 60) 33. Add EMI Solution on USB connector. (Page 52) 34. Add EMI Solution on HDMI connector. (Page 48) 35. Add EMI Solution on IO connector. (Page 65) 36. Add EMI Solution on HDD connector. (Page 51) 37. Add EMI Solution on T/P connector. (Page 31)
2008/05/02	38. Correct the Headphone Jack Detect schematic. (Page 98) 39. Change capacitor to MLCC. (Page 33)
2008/05/04	40. Add over-clock strapping. (Page 29)
2008/05/06	41. Reserve Finger Printer Schematic. (Page 63) 42. Add Amplifer strapping. (Page 37) 43. Remove the Capacitor of headphone. (Page 37)

2008/11/17	3. Add comment for supporting Quad Core CPU. (Page 3) 4. Reserve R0411 for support Quad Core, Add BOM option for DC/QC. (Page 4) 5. Add comment for DC/QC. (Page 5) 10. Add comment for DC/QC. (Page 10) 20. Add comment for delete Modem function. (Page 20) 21. Add comment for BOM option. (Page 21) 29. Add comment for CLK Gen BOM option. (Page 29) 30. Change: add Keyboard_LED conntrol signal. (Page 30) 31. Add keyboard LED Power connector, Add comment for delete CIR BOM option (31) 34. Add BOM option for delete RJ11 (34) 35. Add BOM option for delete Modem function (35) 36. Add BOM option for ALC662 and ALC663 co-lay (36) 38. Add BOM option for supporting Array MIC (38) 44. Add BOM option for supporting Debug Connector (44) 45. Add BOM option for supporting Array MIC (45) 50. Add BOM option for Thermal Sensor for QC and DC (50) 63. Add BOM option for deleting FP function. (63) 68. Add BOM option for deleting OLED connector. (68) 69. Co-using of EC.GPA3 pin, for G50V reserved for controlling GAME_LED#. (69)
2008/11/24	31. Change J3103 Pin5, 6 GND name from GND_POWER to GND. (31) 30. Change net GAME_LED_EC# from connecting with EC.GPA3 to EC.GPA6.(30) 68. Delete all the content of page 68: OLED Connector.(68)
2008/11/25	21.Add TP to USBP9N/P.(21) 45.Add F4502 to protect the M/B from demaging by AC_BAT_SYS_INV short to GND; Change C4513 from 0.1UF/16V to 0.1UF/25V.(45) 2008-11-25-21-06
2008/11/26	14.Change C1447 from 0805 to 0603 to satisfy the mechanical height constrain.(14)
2008/12/31 2009/1/2	80.Change power solution, related page is 80-84, 86, 90-94 60.Replace D6002,D6003,D6004 with integrated D6002 for improving the rise time 70.Reserve R7007 for AMD M96 VGA card 33.Add R3323 to reduce the LAN power consumption ? 36.Change MIC_VREFOUT and 4.7k ohm pull high resistor from page98 to page36, related page is 98, 65, 36
2009/1/4	98.isolate the GND_AUDIO and GND_IO 23.Follow Intel DG R2.2, change C2301 from 0.1UF/16V X7R-->1UF/10V X5R 38.change the DSP VDD power to +1.5VS for better immunity of noise and less power 31.change the keyboard connector pin define for chocolate keyboard
2009/1/8	21.Swap USB port 4 and 8, Camera use port 8, newcard use port 4, to decrease the EMI of camera when USB HDD is also used
2009/1/13	80.power team update the schematic 31.Keyboard signal swap for capacitor layout 30.Change EC pin GPH3/ID3 from BAT_LEARN to T3011, delete BAT_LEARN signal 80,81,84. Add net CLK_EN#; Change U8101 symbol; Add R8404 31.Keyboard connector signal change back

G60VX R1.2

2009/03/05	Page 23: R2319, R2320 change to 100 ohm (Follow Intel DG R2.2) Page 32: Reserve Force_off# connect to EC_RST# page 41/42: Reserve 10pf capacitor for SD card CLK for EMI Page 43: Add MOS to prevent the leakage current from +3VSUS (U4301 pin 17) to BUF_PLT_RST# page 45: Reserve 33pf capacitor for PWR_LED#, GAME_LED# for EMI Page 45: Change R4501, mount C4503 to tune the falling time of +3VS_LCD Page 46: Follow M52V to change the schematic of RGB to tune the rise/fall time Page 46: Add schematic to protect the HSYNC/VSYNC from pulling low by CRT connector for M52VP Page 48: Reserve schematic for G50VX HDMI HPD signal level shift Page 48: Reserve pull high resistor and decoupling capacitor for TMDS signals Page 53: change WLAN pin 39,41 from NC to 3.3V power for full support Intel WiFi Link Page 69: Change GAME_LED# control from PIC MCU to EC Page 70: Reserve bead for MXM card for EMI Page 81: Reserve D8107 to prevent leakage from +3V, +3VS to +3VSUS and ENBL when VSUS_ON accidentally pulled low Page 98: Reserve VPORT (varistor) on signal HP1_IN#_IO and JACK_IN#_IO for ESD protection
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PEGATRON		Title : System History 2	
Pegatron BU2 HW Team 3		Engineer: Kevin1_Guo	
Size	Project Name		Rev
Custom	G60VX		R 1.2
Date: Thursday, March 12, 2009		Sheet	100 of 100